Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

Enhancing High-Performance Computing: A Comprehensive Study on Dual-Doped Source/Drain Reconfigurable Field Effect Transistor

Z. Ahangari *

Department of Electronic, Yadegar- e- Imam Khomeini (RAH) Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.

Article Info

Article History:
Received 15 March 2024
Reviewed 20 April 2024
Revised 01 June 2024
Accepted 26 June 2024

Keywords:
Reconfigurable field effect transistor
Multi-Doped source/drain
Gate workfunction
Logic gate

*Corresponding Author's Email Address:
z.ahangari@gmail.com

Abstract

Background and Objectives: In this study, a reconfigurable field-effect transistor has been developed utilizing a multi-doped source-drain region, enabling operation in both n-mode and p-mode through a simple adjustment of electrode bias. In contrast to traditional reconfigurable transistors that rely on Schottky barrier source/drain with identical Schottky barrier height, the suggested device utilizes a straightforward fabrication process that involves physically multi-doped source and drain. The proposed structure incorporates a bilayer of n^+ and p^+ in the source and drain regions.
Methods: The device simulator Silvaco (ATLAS) is utilized to conduct the numerical simulations.
Results: The transistor exhibits consistent transfer characteristics in both modes of operation. The influence of key design parameters on device performance has been analyzed. A notable aspect of this transistor is the integration of an XNOR logic gate within a single device, rendering it suitable for high-performance computing circuits. The findings indicate that on-state currents of 142 µA/µm and 57.2 µA/µm, along with on/off current ratio of 8.68×10^7 and 3.5×10^7, have been attained for n-mode and p-mode operation, respectively.
Conclusion: A single-transistor XNOR gate design offers potential advantages for future computing circuits due to its simplicity and reduced component count, which could lead to smaller, more energy-efficient, and potentially faster computing systems. This innovation may pave the way for advancements in low-power and high-density electronic devices.

This work is distributed under the CC BY license (http://creativecommons.org/licenses/by/4.0/)

Introduction

The scaling of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) and advancements in the complementary metal-oxide-semiconductor (CMOS) industry play a crucial role in the progression of high-performance computing and logic gate technologies. This advancement is typically linked with higher operation frequencies, reduced power consumption, and lower cost per unit. Nevertheless, it also brings about certain challenges such as leakage current, short-channel effects, dopant impurities, and interconnect delays [1]-[3]. Overcoming these obstacles is essential for the continual enhancement of high-performance computing technologies. More complex structures like FinFETs and silicon-on-insulator (SOI) devices have been introduced as substitutes for traditional CMOS devices [4]-[7]. Nevertheless, the challenge persists in terms of the requirement for expensive processing technology and the continuous pursuit of enhancing transistor density on a chip.

Reconfigurable field effect transistors (RFET) have been proposed as an innovative alternative to traditional MOSFETs, offering the ability to switch between n-mode and p-mode operations by adjusting the bias of their

electrodes without the need for additional doping [8]-[12]. This enhanced flexibility enables a wide range of applications compared to the fixed operation mode of MOSFETs. Unlike the impurity doping used in classical CMOS to define polarities in the channel, source and drain regions, reconfigurable transistors utilize electrostatic doping to regulate carrier injection through Schottky barriers at the source and drain. In n-mode, the transistor acts as an electron-rich semiconductor, facilitating current flow between the source and drain. Conversely, in p-mode, the transistor functions as a hole-rich channel, enabling current flow in a different manner. The operational flexibility of reconfigurable transistors provides numerous advantages over MOSFET-based logic gates, including functional flexibility, optimized power consumption, adaptability to various applications, and simplified design processes.

The RFET operates based on two gates, the control gate and the program gate. The control gate controls the device on and off state, while the program gate modulates the band bending to determine which type of carrier (electron or hole) can flow from the source to the drain along the channel. It is crucial for both n-mode and p-mode operations to have identical transfer characteristics. This requires a nearly equal Schottky barrier height for both electrons and holes. In the case of a Silicon channel material, Nickel Silicide ($NiSi_2$) is used as the source/drain Schottky contact, providing a Schottky barrier height of 0.59 eV for electrons. Considering the silicon band gap value of 1.12 eV, a Schottky barrier height of 0.53 eV can be achieved for holes [13]. Experimental investigations on the electrical characteristics of a nanowire RFET have shown near-symmetric transfer characteristics. The utilization of multi-gate RFETs in circuit design has been explored to enable the development of multi-stage digital circuits with two threshold voltages [14]. Additionally, various RFET structures have been implemented using SiGe [10] and two-dimensional materials [15]-[16]. Reconfigurable transistor based on extended source configuration is presented in [17], where the $NiSi_2$ Schottky contact of the source is extended across the channel region to enhance the tunneling area. As a consequence, this modification leads to an increase in the off-state current. The impact of the position of the control gate and program gate on the efficiency of the Schottky barrier RFET is examined. The findings indicate that when tunneling happens at the junction of the source and channel areas, decreasing the spacer length in the source region leads to an increase in the on-state current [18]. In [19], a logic gate utilizing Schottky source-drain RFET technology is described. The gate architecture involves the integration of multiple transistors to facilitate the construction of both NAND and NOR gates. In the context of neural network applications, the utilization of a XNOR logic gate that relies on a metal source-drain structure is examined [20].

One of the main challenges of RFET is adjusting the Schottky barrier height to ensure identical n-mode and p-mode operation across different materials. Fermi level pinning poses a significant challenge by keeping the Schottky barrier height independent of the metal workfunction. In [21], a novel reconfigurable field effect transistor is introduced, which is based on a dual doped source/drain region. This device incorporates three gates, including two program gates located at the interface of the source and drain regions, and a control gate positioned in the middle of the channel. Furthermore, the device features a floating gate that serves as a charge storage element, enabling seamless switching between the n-mode and p-mode. However, limitation of this study is the necessity of high voltage for programming the device and storing charges. Additionally, the device requires the accumulation of opposite charges to transition from the n-mode to the p-mode, thereby limiting its dynamic switching capabilities. The feasibility of 3D dual doped RFET is considered in [22]. In [23], the proposed reconfigurable transistor has asymmetric structure. The source region is dual doped while the drain region is Schottky contact. However, the use of Schottky contacts in RFET devices is limited by the requirement for nearly equal Schottky barrier heights to achieve identical behavior in both n-mode and p-mode operation. This restriction hinders the exploration of alternative materials for this device structure, as the Schottky barrier height is typically dependent on the material used. This limitation restricts the use of different materials for the device, which can limit its potential performance and scalability. In contrast to the conventional RFET as described in [24], the program gate is situated at the source side while the control gate is positioned at the drain side. This particular arrangement serves to decrease the subthreshold swing of the device; however, the positioning of the control gate at the drain side renders it vulnerable to fluctuations in drain bias. The analog performance of the device with dual doped source and drain regions is considered in [25]. The device shows identical characteristic with respect to the Schottky barrier RFET. Different techniques for inducing negative differential resistance (NDR) region in the transfer characteristic of the RFET is investigated [26]. In [27], an RFET device containing three gates within the device structure is investigated. The two program gates are situated at the boundary between the source and channel regions, while the control gate is positioned centrally within the channel. Through the manipulation of the bias voltages applied to these gates, modulation of the charge density in the channel is achieved, leading to band-to-band tunneling occurring at the center of the channel.

The device is capable of functioning in both the TFET and conventional MOSFET modes. The drain current of the device is particularly affected by variations in the gate bias values, with higher gate bias utilized for charge accumulation.

In this study, a double gate dual-doped RFET (DDRFET) is proposed, where Silicon material is used in the source and drain regions instead of Schottky contacts. To achieve reconfigurable operation, half of the source region is doped n^+ and the other half is doped p^+. This novel structure demonstrates consistent behavior for both n-mode and p-mode operations. The device is equipped with two control gates, namely the program gate and the control gate, which play a crucial role in regulating the flow of carriers from the source to the channel. The impact of geometrical design parameters on the device performance is thoroughly evaluated. Basically, the proposed double gate architecture is more scalable than 3D FinFETs due to its ability to maintain the double gate structure even at smaller dimensions. This allows for more aggressive scaling while maintaining performance and reducing power consumption. The employment of a dual doped configuration in the source and drain region enhances the feasibility of utilizing this device with various materials.

The main focus of this research is the absence of Schottky contacts in the source and drain regions, eliminating the need for a spacer region to isolate the gate and source electrodes. This configuration allows for optimal gate controllability at the interface between the source and channel region. Additionally, the proposed DDRFET structure incorporates the XNOR logic gate utilizing a single transistor. The control gate and program gate values are designated as inputs, while the drain current level serves as the output. An essential characteristic of the XNOR gate designed with a dual doped device in comparison with Schottky barrier RFET is the drain current insensitivity to the Schottky barrier height for both electrons and holes. This paper opts for low gate bias settings for the gates, resulting in the operation of the device solely in the MOSFET mode and distinct current levels being observed. The XNOR gate design presented in this research, which relies on the level of drain current, enables the efficient implementation of logic operations within the device. The manuscript is structured in the subsequent manner: the configuration of the device and simulation models are presented in the succeeding section. Subsequently, findings concerning the influence of design parameters on the performance of the suggested DDRFET are discussed, along with the truth table of the designed logic gates. To conclude, a summary of the paper is provided in the concluding section.

Device Structure and Simulation Models

Fig. 1 illustrates the 2D diagram of the proposed reconfigurable Field-Effect Transistor (FET) that utilizes dual doped source/drain regions. The source and drain regions consist of a bilayer heavily doped p^+-n^+ junction. This device incorporates two distinct gate electrodes, which are separated by an insulating region. The control gate (V_{CG}), positioned in close proximity to the source region, is responsible for both the operational on and off states of the device, as well as the modulation of the potential barrier at the interface of the source and channel region. On the other hand, the program gate (V_{PG}) controls the band bending and determines the type of carrier that flows, whether it operates in the p-FET or n-FET mode. The p^+ and n^+ bilayers in the source and drain regions possess equal potential (zero volt in the source region and V_{DS}=1V in the drain region), effectively preventing band to band tunneling in these regions. When the control gate and program gate have a positive value, the device functions in the n-mode. In this mode, the control gate adjusts the potential barrier at the interface between the n^+ source and the channel. As a result of the accumulation of electrons in the channel, a high potential barrier forms at the interface of the p^+ source. This barrier prevents the flow of holes in the channel. Conversely, when the control gate and program gate have a negative value, the device operates in the p-mode. In this mode, the control gate modulates the potential barrier at the p^+ source, subsequently blocking the flow of the opposite charge from the n^+ source.

The initial design parameters are summarized in Table 1.

Table 1: Initial design parameters of the proposed DDRFET

Parameter	Value
Workfunction of the control gate	4.7 eV
Workfunction of the control gate	4.7 eV
Channel thickness	10 nm
Channel length	150 nm
Length of control gate	70 nm
Length of program gate	70 nm
Spacer length	10 nm
Channel doping density	Intrinsic
n^+ source/drain doping density	10^{19} cm^{-3}
p^+ source/drain doping density	10^{19} cm^{-3}
Gate oxide thickness (hfo_2)	1 nm

Silvaco device simulator [28] is utilized to conduct numerical simulations, and the simulator incorporates the following models: (a) Drift and diffusion model; The device operates on the principle of modulating the potential barrier at the interface between the source and channel region through the control gate bias. The drift current is generated as a result of carriers moving in

response to an electric field, while the diffusion current is caused by the transportation of charges due to the non-uniform concentration of charged carriers in a semiconductor material. (b) Auger and Shockley-Read-Hall (SRH) recombination models have been developed to provide a comprehensive understanding of the impact of recombination and the generation of carriers on carrier transport in the presence of defects and traps. (c) Mobility Models; The carrier drift velocity, which plays a crucial role, is greatly affected by carrier mobility. The simulation considers the impact of both horizontal and vertical electric fields on carrier mobility, utilizing relevant models. Moreover, the presence of dopants as impurities negatively affects carrier mobility, resulting in a decrease in velocity due to scattering [29]-[30]. Mobility models that incorporate the influence of dopants are also integrated. (d) Quantum Confinement Model; The Quantum Confinement effect is primarily observed in thin channel thicknesses, resulting in energy sub-bands characterized by elevated energy levels confined within the channel [31]-[33]. (e) The band-to-band tunneling model is utilized to describe the phenomenon of carriers tunneling at the interface of the n^+-p^+ region. It is important to highlight that the n^+-p^+ in the source and regions possess identical potential. Consequently, there is no carrier transport across the dual doped regions.

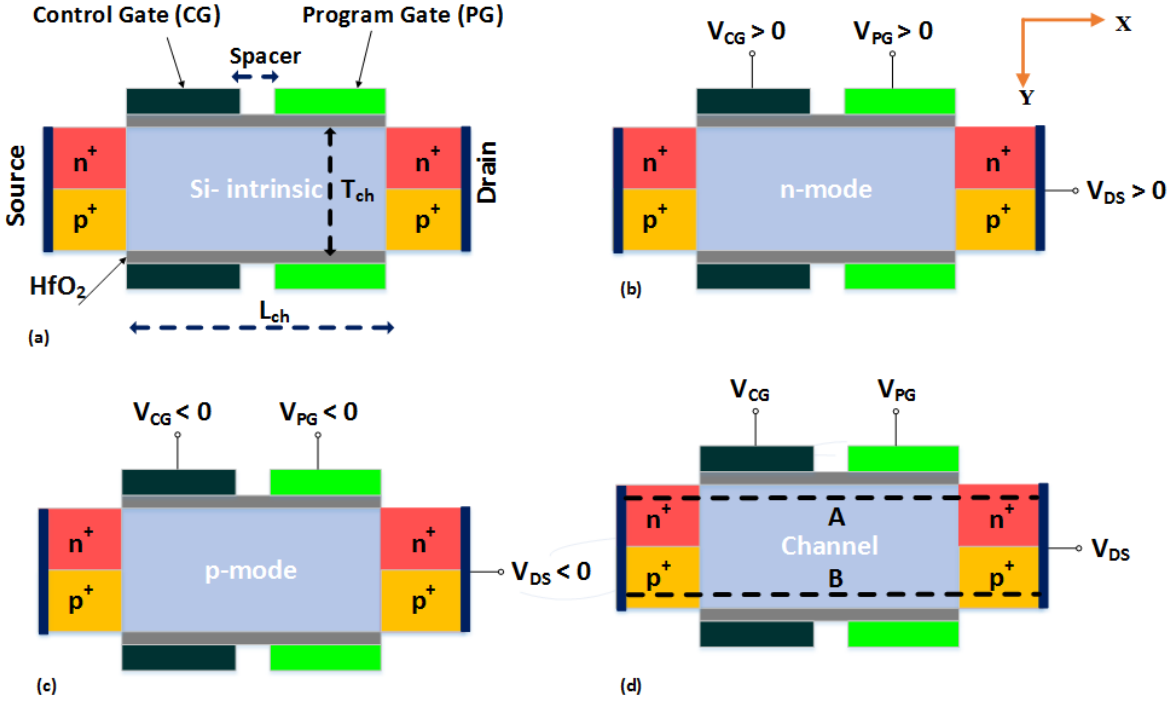

Fig. 1: (a) 2D schematics of the proposed DDRFET, (b) n-mode operation of the DDRFET, (c) p-mode operation and (d) cutline along which the energy bands are illustrated.

Results and Discussion

The distinguishing characteristic of the DDRFET is its ability to operate in both the n-mode and p-mode simply by adjusting the bias values of the control gate, program gate, and drain electrodes. This is made possible by the presence of dual doped n^+ and p^+ source and drain regions, which allow the necessary carriers to move through the device. In the n-mode operation, where all the electrodes have positive values, electrons accumulate in the channel, enabling the flow of n^+ source carriers from source to drain. Conversely, the accumulation of electrons in the channel creates a high potential barrier at the interface of the p^+ source and channel, preventing the flow of holes in the channel. Similarly, when the electrodes are negatively biased, holes accumulate in the channel, resulting in a low potential barrier at the interface of the p^+ source and channel. This facilitates the flow of holes through the channel. At the same time, a high potential barrier is formed at the interface of the n^+ source and channel, hindering the movement of carriers with opposite charge.

Fig. 2 displays the energy band diagram of the DDRFET in both the off-state and on-state for n-mode operation from the n^+ source and p^+ source. In the off-state for n-mode operation, shown in Fig. 2 (a), the electrodes are biased as follows: V_{CG}=0V, V_{PG}=1V, and V_{DS}=1V. The energy band diagram from the n+ source shows a high potential barrier at the interface of the n^+ source and channel region due to the absence of the control gate. As

illustrated in Fig. 2 (b), the energy band in the off-state from the p+ source indicates a high potential barrier for holes to flow. In this case, only minority carriers from the p^+ source region contributes to the current. As the control gate bias increases towards positive values, depicted in Fig. 2 (c), electrons accumulate in the channel, gradually reducing the potential barrier at the interface of the n+ source and the channel region. It is important to note that the program gate alters the energy band bending at the drain side, facilitating the electron flow from source to drain. Conversely, as, depicted in Fig. 2 (d) the accumulation of electrons in the channel increases the potential barrier at the p+ source side, hindering the flow of holes in the channel.

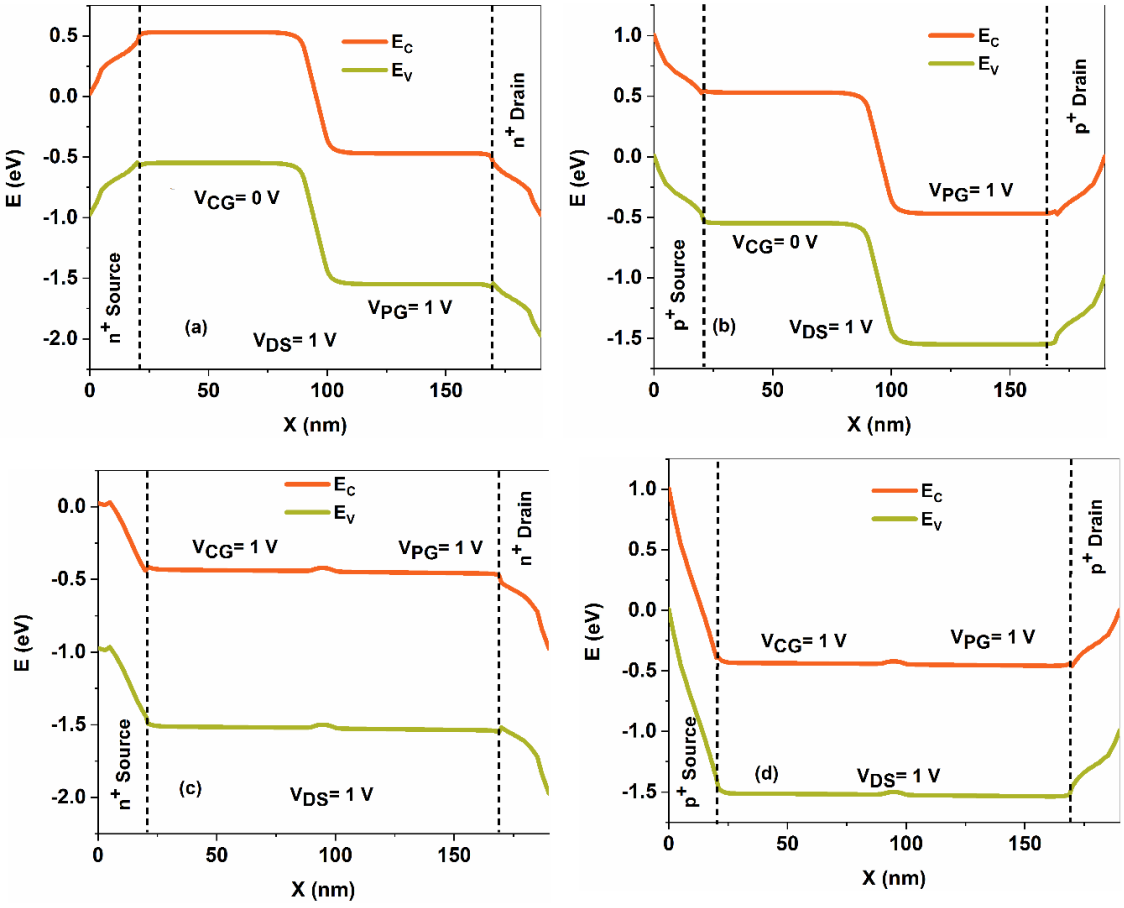

Fig. 2: Energy band diagram of DDRFET in the n-mode operation along the device from source to drain in (a) off-state condition from the n^+ source to n+ drain (cutline along the A direction), (b) off-state condition from the p^+ source to p^+ drain (cutline along the B direction), (c) on-state condition from the n^+ source to n^+ drain (cutline along the A direction), and (d) on-state condition from the p^+ source to p^+ drain (cutline along the B direction).

Similarly, the band diagram of the proposed DDRFET for p-mode operation from the n^+ and p^+ source is presented in Fig. 3. In Fig. 3 (a), under off-state conditions with V_{CG}=0V, V_{PG}=-1V, and V_{DS}=-1V, the band bending near the drain region in the channel is a result of the program gate that blocks the flow of electrons in the channel. In addition, a high potential barrier is created at the n+ source-channel interface and only minority carriers from the n+ source region contributes to the off-state current. Furthermore, Fig. 3 (b) shows a high potential barrier at the channel-p^+ source interface that hinders hole flow in the channel. Transitioning to the on-state by increasing the control gate voltage to negative values leads to hole accumulation in the channel, impeding electron flow from the n^+ source, as depicted in Fig. 3 (c). Nevertheless, the accumulated holes in the channel facilitate hole transport from the p^+ source region towards the drain, as illustrated in Fig. 3 (d).

Fig. 4 depicts the transfer characteristics of the DDRFET, showcasing its performance in both n-mode and p-mode operation. Notably, the device exhibits a nearly symmetrical behavior for both modes.

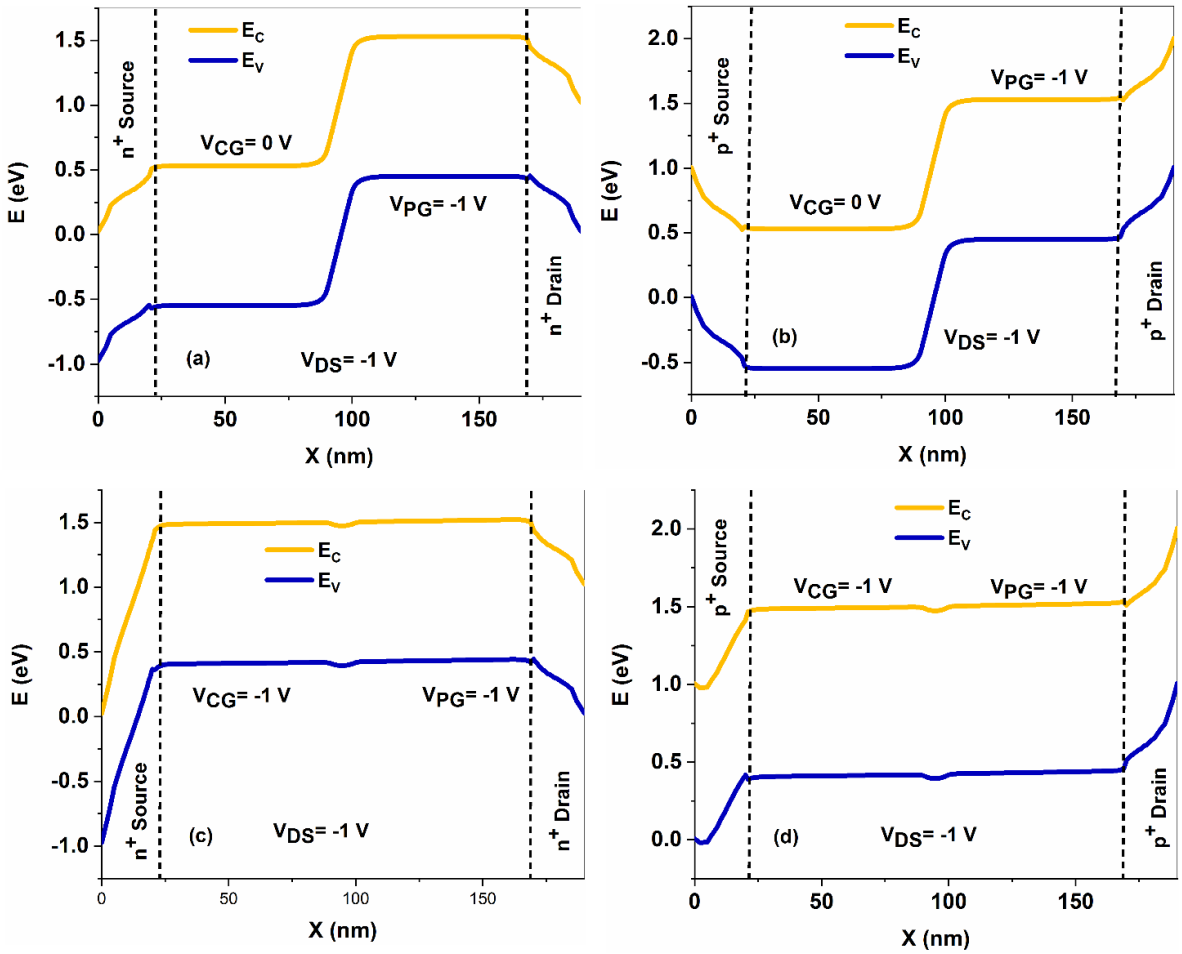

Fig. 3: Energy band diagram of DDRFET in the p-mode operation along the device from source to drain in (a) off-state condition from the n^+ source to n+ drain (cutline along the A direction), (b) off-state condition from the p^+ source to p^+ drain (cutline along the B direction), (c) on-state condition from the n^+ source to n^+ drain (cutline along the A direction), and (d) on-state condition from the p^+ source to p^+ drain (cutline along the B direction).

In the case of n-mode operation, it achieves an on-state current of 142 µA/µm, an on/off current ratio of 8.68×10^7, threshold voltage of 0.23 V and a subthreshold swing of 64.7 mV/dec. Similarly, for p-mode operation, the DDRFET attains an on-state current of 57.2 µA/µm, an on/off current ratio of 3.5×10^7, threshold voltage of -0.301 V and a subthreshold swing of 80.2 mV/dec. By definition, threshold voltage is the control gate bias level at which a drain current of 10^{-8} A/µm is attained. The gate workfunction plays a crucial role in the design of the device, significantly impacting its performance. In principle, the DDRFET functions by altering the polarity of the electrodes to achieve comparable transfer characteristics for both n-mode and p-mode operations. The difference in workfunction between the gate and the channel effectively controls the carrier density within the channel. Fig. 5 demonstrates how variations in gate workfunction affect the performance of the DDRFET in both n-mode and p-mode operations. The findings indicate that lower gate workfunction values lead to a significant increase in electron density in the channel during the off-state, resulting in higher off-state current in n-mode operation. In p-mode operation, a higher negative bias is needed initially to deplete the accumulated electrons in the channel, leading to an increase in the threshold voltage for the onset of p-mode operation. Increasing the gate workfunction reduces the electron density in the channel, thereby decreasing the off-state current. Conversely, in p-mode operation, an increase in hole density in the channel enhances the on-state current. To ensure optimal device performance, it is essential to achieve similar transfer characteristics with nearly identical threshold voltages. The study suggests that a gate workfunction value of 4.7 eV is optimal for achieving the lowest off-state current of 1.63×10^{-12} A/µm and threshold voltages of 0.23 V and -0.301 V for n-mode and p-mode operations, respectively. Beyond this optimal value, an increase in gate workfunction leads to higher hole density in the channel, resulting in increased off-state current in p-mode operation, while a reduction in electron density in n-mode operation leads to an increase in threshold voltage.

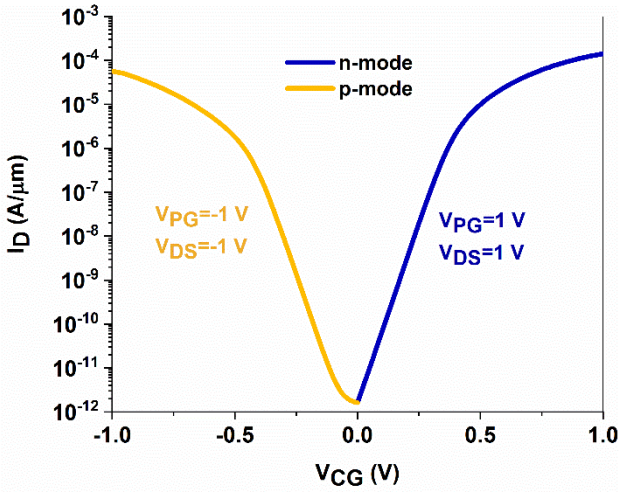

Fig. 4: Transfer characteristics of DDRFET in the n-mode and p-mode operation.

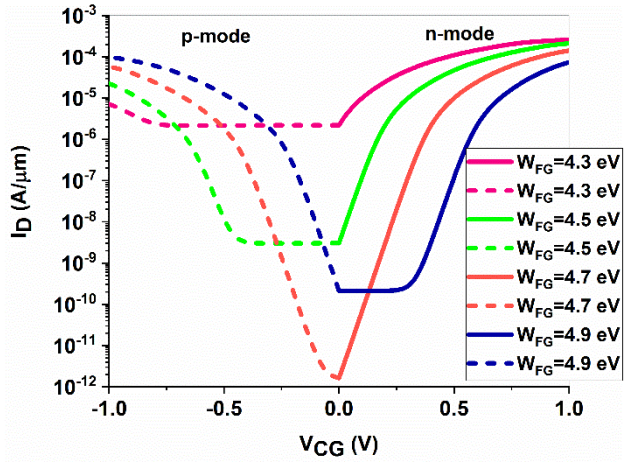

Fig. 5: Transfer characteristics of DDRFET in the n-mode and p-mode operation as the workfunction of the control gate and program gate are parameterized.

Fig. 6 demonstrates the impact of the length of the control and program gate on the on-state current of the DDRFET for n-mode and p-mode operation. When the gate length decreases, a slight decrease in the on-state current is observed due to the increase in parasitic resistance of the uncovered channel region. It is important to note that the off-state current is determined by the potential barrier height at the source-channel interface. The modulation of the potential barrier at the dual-doped source region interface by the control gate results in minimal changes in the off-state current (not depicted).

Fig. 7 depicts the impact of channel thickness on the performance of the proposed DDRFET. It is important to note that, due to the dual-doped source/drain structure, current flows from the source specific doping that matches the majority carrier accumulated in the channel. The findings indicate that as the channel thickness decreases, quantum confinement leads to an increase in energy of the states, resulting in a decrease in the density of states. Furthermore, reducing the source/drain thickness leads to a decrease in the source-channel interface area for carrier transport initiation. It is evident that as the channel thickness decreases, the density of accumulated majority carriers in the channel also decreases.

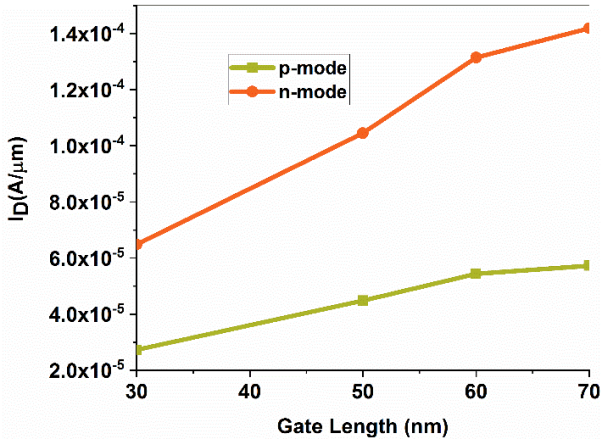

Fig. 6: On-state current of DDRFET in the n-mode and p-mode operation as the gate length is varied.

The 2D contour displayed in Fig. 8 illustrates the variation of drain current in relation to changes in the control gate and program gate. The contour reveals that the highest drain current values are observed in the top-right and bottom-left sections. In the top-right region, both the control gate and program gate exhibit positive values, leading to n-mode operation and maximum drain current output when the control and program gates reach their peak values.

Conversely, when the program gate and control gate are negative, the device operates in p-mode. It is important to note that in p-mode operation, the roles of the drain and source electrodes are reversed, with the drain electrode at 0.05 V and the source electrode at 0 V. On the contrary, when the control gate and program gate are biased oppositely, lower drain current values are anticipated, as shown in the top-left and bottom-right areas of the contour. This behavior is primarily influenced by the program gate, which creates a barrier for carrier transport, hindering the flow of accumulated carriers in the channel controlled by the control gate. A key characteristic of the proposed DDRFET is its ability to function as a logic gate within a single device. The control gate and program gate serve as inputs, while the drain current level functions as the output of the logic gate. A high gate potential of 1.0 V corresponds to logic "1", while a low gate potential of -1.0 V represents logic "0". A drain current below 10^{-12} A/μm signifies logic "0", whereas a drain current exceeding 10^{-8} A/μm indicates logic "1". The drain current remains constant at V_{DS}=0.05 V. Table 2 displays the truth table for the suggested logic gate.

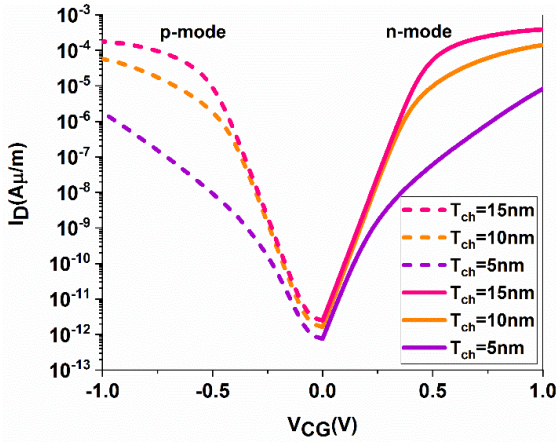

Fig. 7: I_D-V_{CG} curves of DDRFET in the n-mode and p-mode operation as the channel thickness is varied.

Table 2: Truth table of the proposed XNOR gate implemented by the proposed DDRFET

V_{CG}	V_{PG}	on-state current
0	0	**1**
0	1	**0**
1	0	**0**
1	**1**	**1**

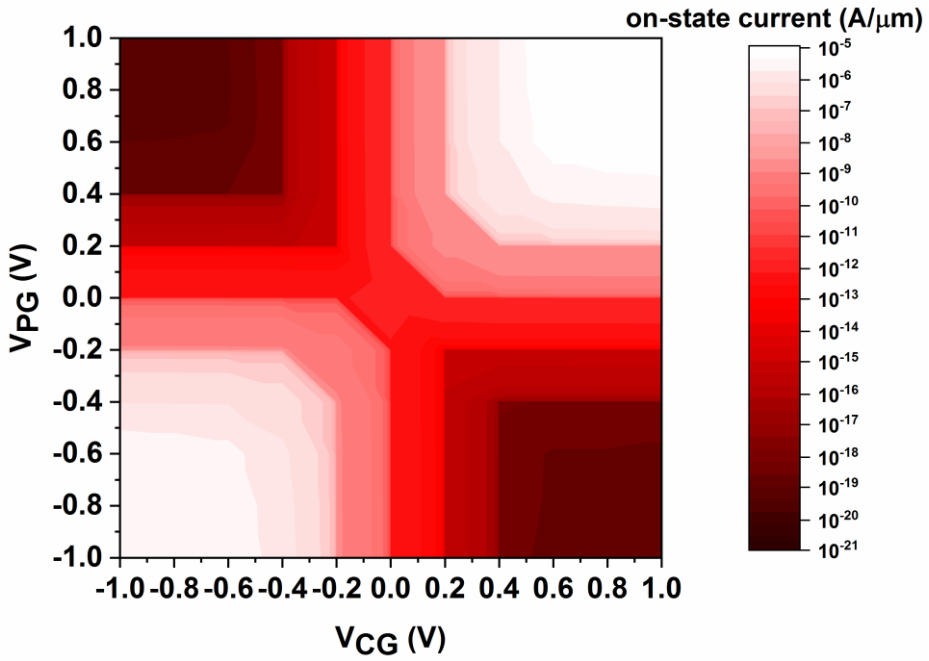

Fig. 8: 2D variation matrix of on-state current as the control gate and program gate bias is varied.

The influence of temperature on the device performance for n-mode and p-mode operation is illustrated in Fig. 9. The findings indicate that the off-state current of the device is significantly influenced by changes in temperature, attributed to the presence of increased energy carriers at elevated temperatures. Conversely, the saturation current of the device, which is controlled by the gate bias, remains unaffected by temperature variations.

The impact of drain bias on the transfer characteristics of the DDRFET being considered is illustrated in Fig. 10. The device demonstrates a minimal sensitivity of the off-state current to changes in the drain electric field, resulting in significant resistance to drain bias even with a reduced channel length. It is apparent that the rise in on-state current is attributed to the heightened carrier velocity observed at elevated drain voltages.

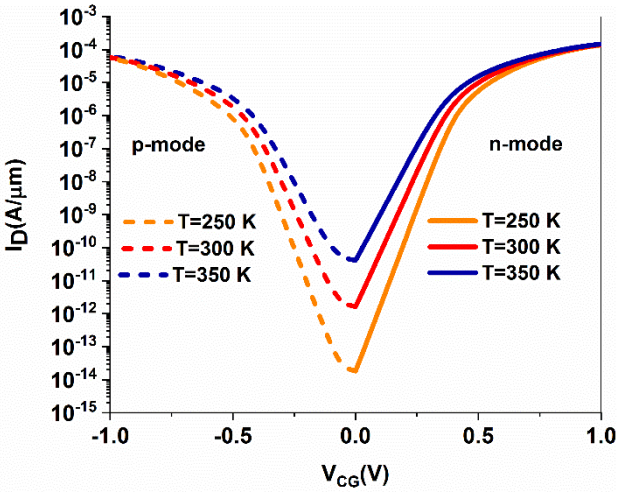

Fig. 9: I_D-V_{CG} curves of DDRFET in the n-mode and p-mode operation as the temperature is parametrized.

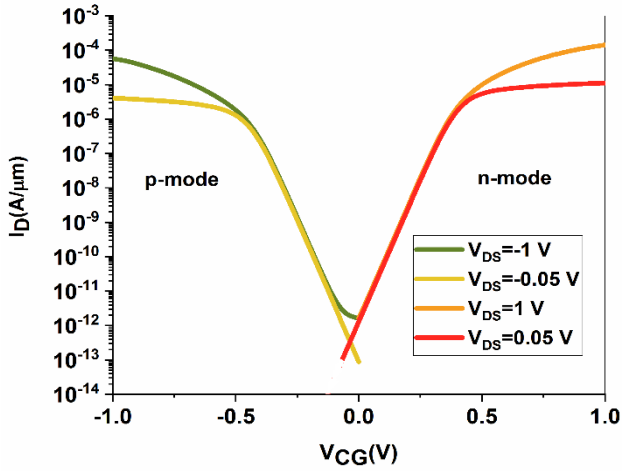

Fig. 10: Transfer characteristics of DDRFET in the n-mode and p-mode operation as the drain bias is parametrized.

Conclusion

The electrical properties of a reconfigurable field effect transistor are thoroughly examined in this study, utilizing multi doped source and drain regions. The findings indicate that the gate workfunction plays a crucial role in effectively controlling the channel charge density. To achieve similar transfer characteristics for both n-mode and p-mode operations, it is imperative to determine the optimal value for the gate workfunction. The length of the control gate and program gate has minimal impact on the device's performance, whereas extremely thin film channel thicknesses negatively affect the device on-state current. A key aspect of the proposed design is the integration of an XNOR gate within a single device, which simplifies the creation of high-speed computing circuits.

Author Contributions

Z. Ahangari discussed, simulated the results and contributed to the final manuscript.

Acknowledgment

The author would like to thank the editor and anonymous reviewers.

Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistors
CMOS	Complementary Metal-Oxide-Semiconductor
RFET	Reconfigurable Field Effect Transistor
DDRFET	Dual-Doped Reconfigurable Field Effect Transistor
SOI	Silicon on Insulator

References

[1] A. Chaudhry, M. J. Kumar, "Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review," IEEE Trans. Device Mater. Reliab., 4(1): 99-109, 2004.

[2] S. H. Noh et al., "Improvement in short-channel effects of the thin-film transistors using atomic-layer deposited In--Ga--Sn--O channels with various channel compositions," IEEE Trans. Electron Devices, 69(10): 5542-5548, 2022.

[3] P. Arul, K. Helen Prabha, "A comprehensive analysis of short channel effects on carbon nano tube field effect transistors," J. Nanoelectron. OptoElectron., 16(12): 1905-1912, 2021.

[4] R. K. Maurya, B. Bhowmick, "Review of FinFET devices and perspective on circuit design challenges," Silicon, 14(11): 5783-5791, 2022.

[5] A. Razavieh, P. Zeitzoff, E. J. Nowak, "Challenges and limitations of CMOS scaling for FinFET and beyond architectures," IEEE Trans. Nanotechnol., 18: 999-1004, 2019.

[6] S. Kallepelli, S. Maheshwaram, "A novel circular double-gate SOI MOSFET with raised source/drain," Semicond. Sci. Technol., 36(6): 065009, 2021.

[7] N. A. Srivastava, A. Priya, R. A. Mishra, "Analog and radio-frequency performance of nanoscale SOI MOSFET for RFIC based communication systems," Microelectron. J., 98: 104731, 2020.

[8] T. Mikolajick et al., "Reconfigurable field effect transistors: A technology enablers perspective," Solid-State Electron., 194: 108381, 2022.

[9] C. Navarro, S. Barraud, S. Martinie, J. Lacord, M.-A. Jaud, M. Vinet, "Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations," Solid-State Electron., 128: 155-162, 2017.

[10] A. Fuchsberger et al., "Reconfigurable field-effect transistor technology via heterogeneous integration of SiGe with crystalline Al contacts," Adv. Electron. Mater., 9(6): 2201259, 2023.

[11] S. Larentis et al., "Reconfigurable complementary monolayer MoTe2 field-effect transistors for integrated circuits," ACS Nano, 11(5): 4832-4839, 2017.

[12] C. Roemer et al., "Physics-based dc compact modeling of schottky barrier and reconfigurable field-effect transistors," IEEE J. Electron Devices Soc., 10: 416-423, 2021.

[13] F. Fuchs, S. Gemming, J. Schuster, "Electron transport through NiSi2--Si contacts and their role in reconfigurable field-effect transistors," J. Phys.: Condens. Matter, 31(35): 355002, 2019.

[14] J. Zhang, P.-E. Gaillardon, G. De Micheli, "Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs," in Proc. 2013 IEEE International Symposium on Circuits and Systems (ISCAS): 2111-2114, 2013.

[15] W. Fei, J. Trommer, M. C. Lemme, T. Mikolajick, A. Heinzig, "Emerging reconfigurable electronic devices based on two-dimensional materials: A review," InfoMat, 4(10): e12355, 2022.

[16] R. Ranjith, R. Jayachandran, K. J. Suja, R. S. Komaragiri, "Two dimensional analytical model for a reconfigurable field effect transistor," Superlattices Microstruct., 114: 62-74, 2018.

[17] X. Li, Y. Sun, X. Li, Y. Shi, Z. Liu, "Electronic assessment of novel arch-shaped asymmetrical reconfigurable field-effect transistor," IEEE Trans. Electron Devices, 67(4): 1894-1901, 2020.

[18] Y. Yao, Y. Sun, X. Li, Y. Shi, Z. Liu, "Novel reconfigurable field-effect transistor with asymmetric spacer engineering at drain side," IEEE Trans. Electron Devices, 67(2): 751-757, 2020.

[19] G. Galderisi, T. Mikolajick, J. Trommer, "Reconfigurable field effect transistors design solutions for delay-invariant logic gates," IEEE Embedded Sys. Lett., 14(2): 107-110, 2022.

[20] J. H. Bae et al., "Reconfigurable field-effect transistor as a synaptic device for XNOR binary neural network," IEEE Electron Device Lett., 40(4): 624-627, 2019.

[21] X. Jin, S. Zhang, X. Liu, "A dual doping nonvolatile reconfigurable FET," Sci. Rep., 13(1): 5634, 2023.

[22] R. Zhang et al., "Novel 3-D fin-RFET with dual-doped source/drain to improve ON-state current," IEEE Trans. Electron Devices, 69(12): 6569-6575, 2022.

[23] X. Jin, X. Yuan, S. Zhang, M. Li, X. Liu, "Complementary doped source-based reconfigurable Schottky diode as an equivalence logic gate," ACS Omega, 8(25): 23120-23129, 2023.

[24] C. Navarro et al., "Performance of FDSOI double-gate dual-doped reconfigurable FETs," Solid-State Electron., 194: 108336, 2022.

[25] C. Navarro et al., "3D-TCAD benchmark of two-gate dual-doped Reconfigurable FETs on FDSOI28 technology," Solid-State Electron., 200: 108577, 2023.

[26] L. Sa, G. F. R. Sa, J. Sa, J. Cb, A. J. La, "Challenges and opportunities in implementing negative differential resistance mode reconfigurable field effect transistors," arXiv preprint arXiv:2312.08351, 2023.

[27] B. Lu et al., "A novel nanosheet reconfigurable field effect transistor with dual-doped source/drain," Microelectron. J., 147: 106178, 2024.

[28] ATLAS User Manual, Santa Clara, USA: Silvaco International, 2015.

[29] K. M. Liu C. P. Cheng, "Investigation on the effects of gate-source overlap/underlap and source doping gradient of n-type Si cylindrical gate-all-around tunnel field-effect transistors," IEEE Trans. Nanotechnol., 19: 382-389, 2020.

[30] Y. J. Chung, K. A. V. Rosales, K. W. Baldwin, K. W. West, M. Shayegan, L. N. Pfeiffer, "Working principles of doping-well structures for high-mobility two-dimensional electron systems," Phys. Rev. Mater., 4(4): 044003, 2020.

[31] N. Pandey, Y. S. Chauhan, "Analytical modeling of short-channel effects in MFIS negative-capacitance FET including quantum confinement effects," IEEE Trans. Electron Devices, 67(11): 4757-4764, 2020.

[32] S. Liu et al., "Performance limit of gate-all-around si nanowire field-effect transistors: An Ab initio quantum transport simulation," Phys. Rev. Appl., 18(5): 054089, 2022.

[33] R. Quhe et al., "Sub-10 nm two-dimensional transistors: Theory and experiment," Phys. Rep., 938: 1-72, 2021.

Biographies

Zahra Ahangari received her Ph.D. degree in Electrical Engineering-Electronics from Islamic Azad University, Science and Research Branch, in the year 2013. From the year 2004 onwards, Zahra served as a research assistant in the device modeling and simulation laboratory of University of Tehran under supervision of Professor Morteza Fathipour. Currently, she is the faculty member of Electrical Engineering department at Islamic Azad University, Yadegar-e-Imam Khomeini (RAH) Shahr-e-Rey Branch. Zahra's main areas of research are modeling and simulation of nanoelectronic devices, nano sensors, and solar cells.

- Email: z.ahangari@gmail.com
- ORCID: 0000-0002-1095-3150
- Web of Science Researcher ID: AAP-5468-2021
- Scopus Author ID: 26435067300
- Homepage: https://scholar.google.com/citations?user=NuvC9YMAAAAJ&hl=en

How to cite this paper:
Z. Ahangari, "Enhancing high-performance computing: A comprehensive study on dual-doped source/drain reconfigurable field effect transistor," J. Electr. Comput. Eng. Innovations, 12(2): 475-484, 2024.

DOI: 10.22061/jecei.2024.10757.732

URL: https://jecei.sru.ac.ir/article_2137.html