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Research paper

Uncomplicated Dead-time generation Designed for H-Bridge Drivers by Logic Gates Driving Linear Actuators

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Abstract

Background and Objectives: The H-bridge (HB) driver design with high efficiency is one of the most challenging issues in power systems that drive AC/DC loads. HB driver circuit based upon complementary MOSFET type used as a driving system of DC motor, power converters, and battery charger for electrical vehicles. In Driving DC motors, dead-time (DT) generation has been considered a major factor such as preventive power line short-circuits (shoot-through) over high and low-side MOSFETs. In this paper, the HB driver is designed for linear actuators with consideration for the prevention of shoot-through.
Methods: The propagation delay of logic gates are used to postpone the arrival gate drive signal for high/low side MOSFETs resulting in short circuit elimination on the DC source.
Results: As mentioned, logic gates' propagation delay by their values causes interruption between the high and low-side power switches gate drive signal resulting in shoot-through elimination. Although the existence of DT influences the performance of the rotational speed and output torque of a DC motor by increasing the distortion and pulse interval, Linear actuators due to low-velocity linear motion do not require the PWM control, therefore DT has no substantial effect on driver performance.
Conclusion: Simulation and experimental results validate the method proposed in this paper. According to the specifications of the circuit designed in this paper, for loads that do not need rotational speed control, logic gates with proper propagation delay can be chosen to eliminate short circuits in complementary MOS switches without requiring DT compensation methods.

Introduction

Linear actuators are a type of actuator that converts the rotational movement of motors into low-speed linear or straight thrust/traction motions. Linear actuators are perfect for all kinds of applications where inclination, pulling, lifting, or pushing with pounds of force is necessary, particularly in medical equipment such as Electric hospital beds or care facilities that require precision and smooth motion control. In practice, the HB driver was proposed as a power device to drive the inductive load such as a linear actuator [1].

The basic structure of HB is composed of four power transistors such as BJT, IGBT, or MOSFET. This paper uses complementary MOSFETs as power switches to drive the inductive load (Fig. 1). Due to the physical nature of power switches and body diodes, the transition delays are not the same and consequently, they cannot turn on or turn off simultaneously, IRFZ44ZSPbF (t_{on}= 14ns, t_{off}= 33ns) [2], IRF5305 (t_{on}= 14ns, t_{off} = 39ns) [3]. The intrinsic difference in timing characteristics of power switches leads to an essential issue in driving loads by the HB driver

which can be solved by DT duration "1", where t_{off} denotes the turn-off transition of one switch in the inverter leg [4].

$$t_{DT} \geq t_{off} \quad (1)$$

In practice, the difference between MOSFETs timing transitions caused short circuits among the upper and lower power switches in one inverter leg when HB was driven to change the direction of DC motor rotation or stop driving the load. To overcome this problem, an insertion delay, called DT (t_{DT}) [5], between the pulses generated by driving circuitry activates and deactivates the power switches in one branch to ensure safe operation [6], [7]. However, distortion of the output waveform, fundamental current loss [8], [9] and common-mode voltage issues [10] are the effects of DT duration, especially in the case of speed system control with high-frequency carrier and voltage source converters [11]-[13]. Therefore, DT compensation is one of the most challenging issues for the HB driver system [14], [15]. Although DT duration can prevent the breakdown of CMOS transistors in one inverter branch against shoot-through [16], it should be optimized to reduce body diode conduction and reverse recovery loss [17], [18]. In retrospective studies, different optimization methods were proposed to compensate for the DT effects in power converters and speed control systems [19]. In conventional applications, the fixed DT is used to eliminate the shoot-through [20] while the turn-off time of power switches depends on load current because of junction capacitors [21], [22]. Therefore, DT should be adjusted to an optimum value in case of varying load to eliminate shoot-through. Pulse width adjustment and adaptive DT control are the most convenient compensation methods for power electronic converters [23]-[25].

Although more compensation methods with different features were proposed, most of them require complex hardware design and precise information about the zero crossing of the load current in the existence of the noise and the current ripple which is challenging in implementation.

This paper aimed to intrinsically drive linear actuators with slow linear motion without requiring the speed control system or PWM gating signal. The approach used in this paper is based on a single pulse gate driving that the DT effect is not obvious and shoot-through elimination was guaranteed without requiring DT compensation methods. This approach leads to uncomplicated and reduced hardware utilization in HB drivers.

Modeling and Analysis of Proposed H-Bridge Driver

A. Dead-Time in H-Bridge Driver

Short circuits in complementary MOSFET or half-bridge occur when the direction of load current changes due to the gate driving signal. Changing the direction of DC motor rotation or brake state requires driving the gate of High/Low side power switches in which unequal transition delays from ON to OFF or vice versa may lead to the specific time of concurrent Complementary switches conduction resulting in DC source short circuit. In fact, in HB driver design, the gate driving control section included dead time insertion is substantial which shoot-through was eliminated. DT value depends on some characteristics of power switches such as drive current, voltage bias, input capacitance, and body diode conduction [26], [27]. Typical values for transition delays are informed in component datasheets [2], [3], so gate driving control was designed based on DT> t_{off} and referred values.

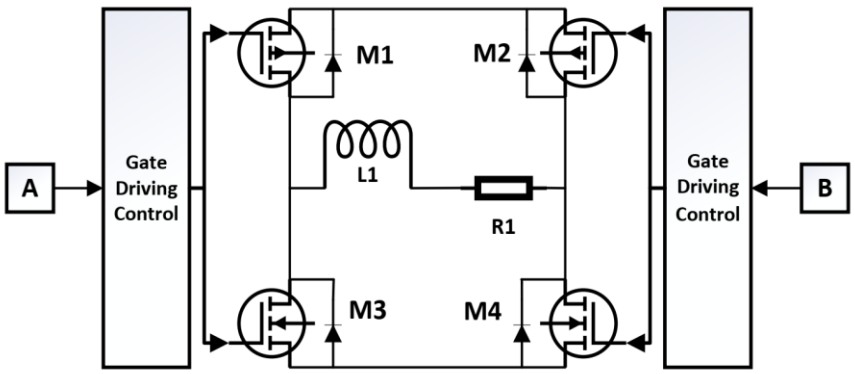


Fig. 1: CMOS H-bridge driver.

Due to the structure of the linear actuators with low-speed linear motion, speed control of the DC motor or PWM signaling is not necessary, therefore DT effects cannot degrade the efficiency of the driver. Furthermore, HB driver simulation (Fig. 2) represented the great importance of DT existence which avoids shoot-through current. The rest of this paper focused on the gate driving control part with the capability of dealing with mismatch transition delay by adding a safety time. Simulation and experimental results are provided to demonstrate the proposed method's validity and performance.

B. Proposed H-Bridge Driver Designing

Sign-magnitude (SM) and lock anti-phase are the most common driving modes in HB drivers. The proposed driver was designed based on the former. In SM mode driving, both CMOS switches are closed in each cycle and the others open.

It is necessary to add dead-time to ensure that one switch is completely off before turning on the complementary switch. In this mode during the off-time, motor winding acts as an inductor ($V_L = L \frac{di_L}{dt}$) which opposes the sudden alteration in current flowing through it. On the other hand, a sudden reduction in its current induces very high range voltages out of power switch limitations, which will destroy them. Therefore, the current should circulate in a motor rotation direction during the off-time which can be accessed by one of the turned-on switches and the other turned-off switch body diode is forward-biased. Inductor-induced voltage rose the Anode of the body diode voltage till its junction is forward-biased. Also, discrete diodes can be used along with CMOS switches instead of body diodes, but two essential characteristics in comparison to body diodes should be considered such as reverse recovery time and forward bias voltage. IRFZ44 (N-Channel) and IRF5305 (P-Channel) were chosen as complementary MOS transistors (Fig. 1). The gate driving circuitry which is comprised of fixed DT generation is incorporated into the proposed HB driver is shown in Fig. 3- 5. As depicted in the driving voltage waveforms (Fig. 4), which fed to power switches and logic gates, two direct-current (DC) potentials provide the desired biasing voltage. The first one is 24-volt which supplies the CMOS gate bias voltages by proper voltage divider resistors and the other is 5-volt which provides logic gates bias voltages. In digital signals, 5-volt generally corresponds to a high signal or '1' binary and zero potential to a low signal or '0' binary. Propagation delays of logic gates cause a blank time between activating and deactivating the CMOS transistors in one leg of the inverter. The High/Low side driver is both composed of two paths to CMOS gates. The path with NAND gates is activated during the turn-on time of the Complementary power switches (Fig. 6).

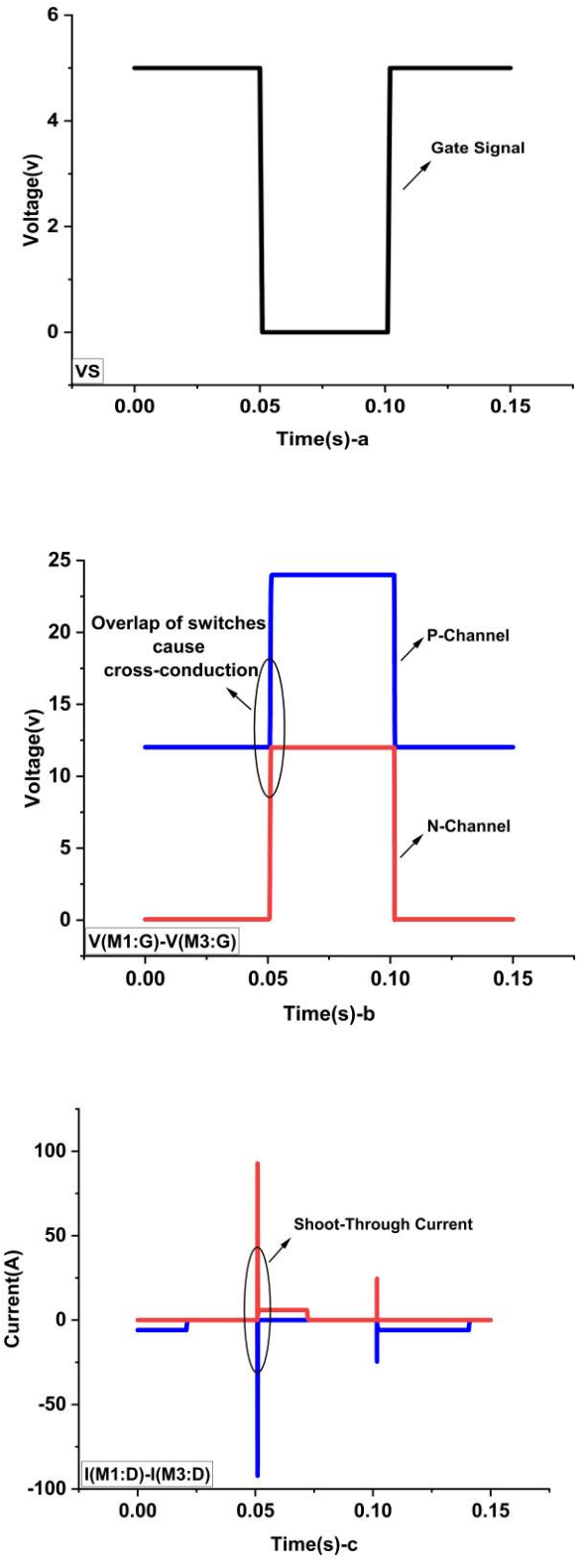


Fig. 2: Short circuit occurred during gate driving of half-bridge without DT; (a) Gate driving signal; (b) Complementary MOSFET's turn on and off concurrently; (c) Short circuit current due to both complementary power switch conduction.

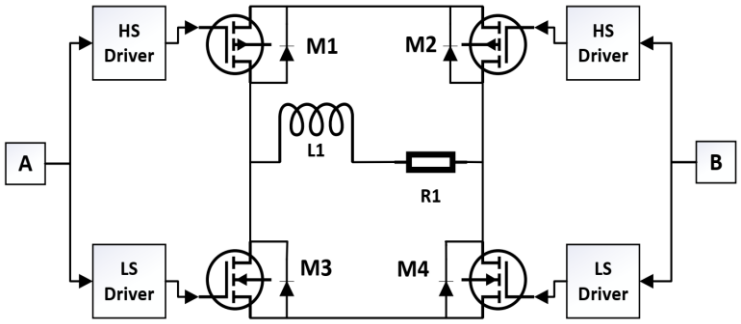


Fig. 3: Block diagram of H-Bridge circuit; HS: High-Side; LS: Low-Side.

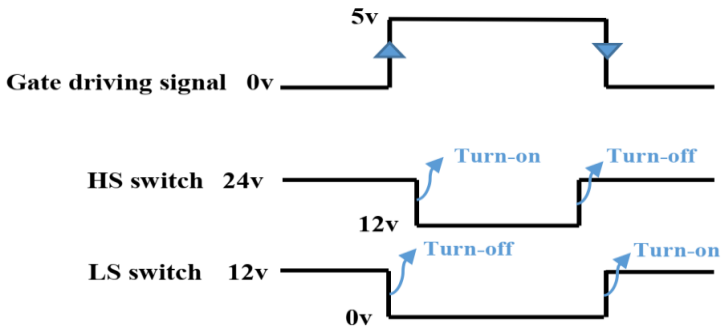


Fig.4: Gate driving signal and the sequence of activation and deactivation of High/Low side switches by the propagation delay of logic gates driving path.

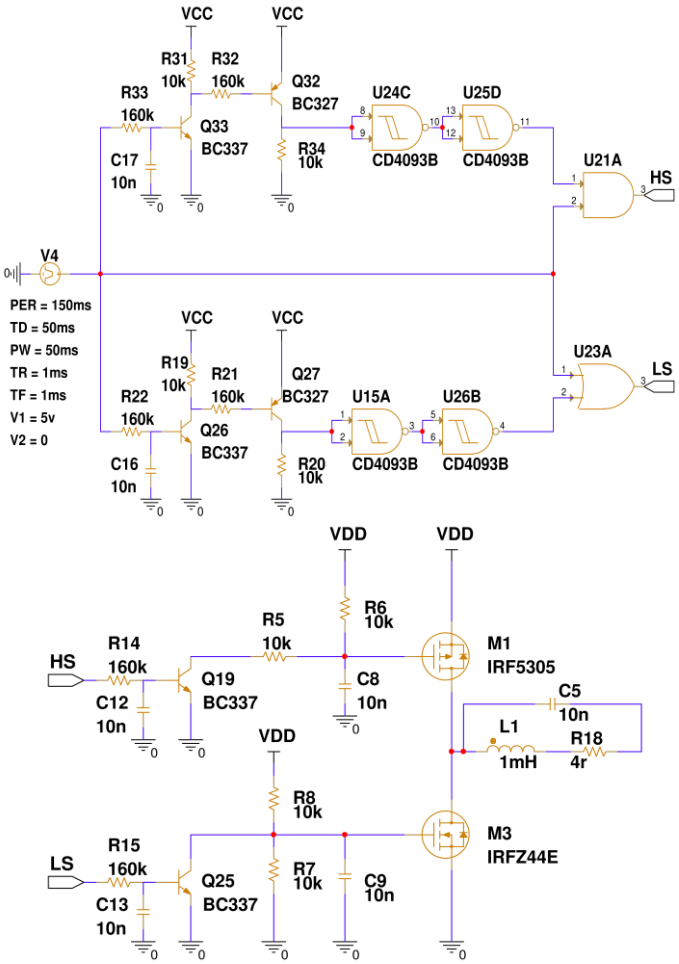


Fig. 5: Schematic diagram of proposed H-Bridge with High/Low side gate driver with NAND gates.

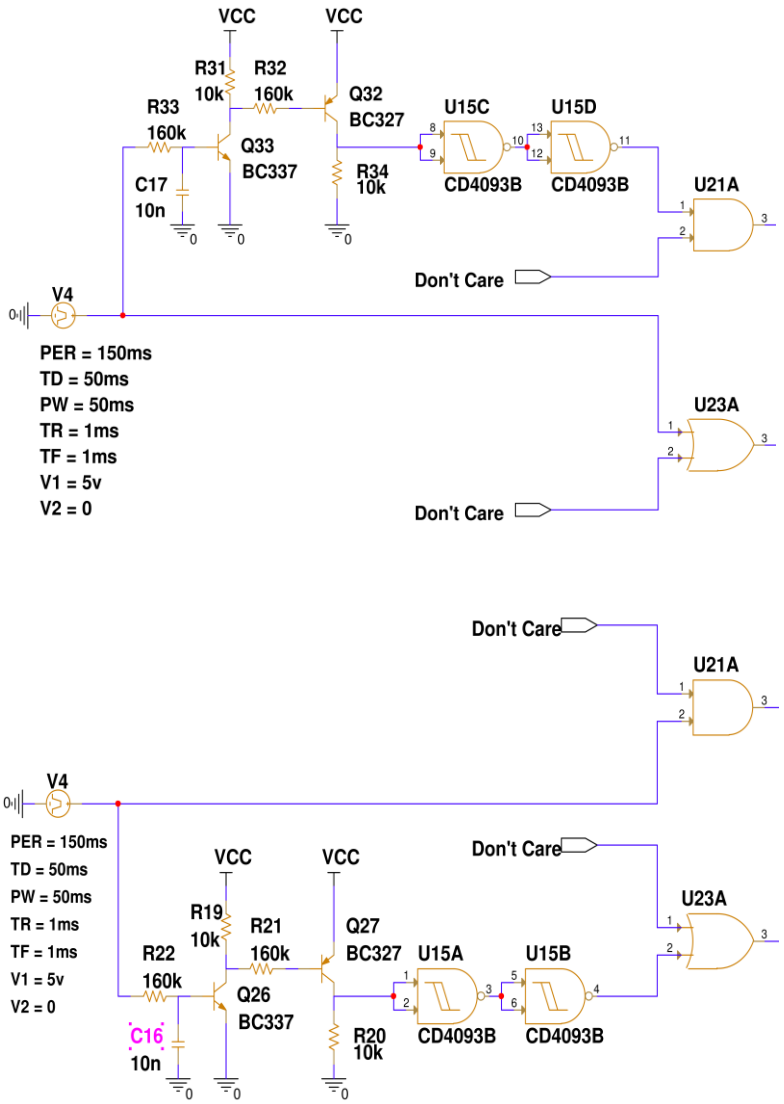


Fig. 6: NAND gates are activated in the turning-on power switch path to postpone the arrival gate drive signal.

This topology confirms one MOS transistor turns off before other complementary transistors turn on due to logic gates propagation delay (PD) acting as DT. As stated by Equ. 1, PD in whole logic gates should be upper than the CMOS turn-off time (IRFZ44: 33ns, IRF5305: 39ns). The rest of the paper is allocated to simulation and experimental results to demonstrate the validity of the proposed method.

Simulation and Experimental Results

The schematic diagram of the proposed H-Bridge in Fig. 5 was simulated in OrCAD Capture CIS version 17.2-2016. Gate driving control as shown in the schematic diagram composed of AND, NAND, and OR Logic gates in the path of high/low side arrival gates drive signal. As illustrated in Fig. 7, the outputs of logic gates level change on the length of the time interval between the specified reference points (V_M) on the input and output voltage waveforms.

These time intervals are called t_{PHL} when output switches from high to low and t_{PLH} when output switches from low to high. t_{PHL} and t_{PLH} act as DT to eliminate CMOS transistor cross-conduction. DT must be higher than the turn-off time of power switches, and the higher value of the turn-off time considered (t_{off}=39ns). According to Fig. 5, three types of logic gates were used to add proper DT in the arrival gate drive signal (Table 1).

Table 1: Types and timing characteristics of logic gates. t_{PLH}: LOW to HIGH propagation delay; t_{PHL}: HIGH to LOW propagation delay

Part Number	Type	Power Supply	t_{PLH}		t_{PHL}		Unit
			Typ	Max	Typ	Max	
HEF4093B [28]	NAND	5v	85	170	90	185	ns
HEF4081B [29]	AND	5v	45	90	55	110	ns
74LS32 [30]	OR	5v	3	11	3	11	ns

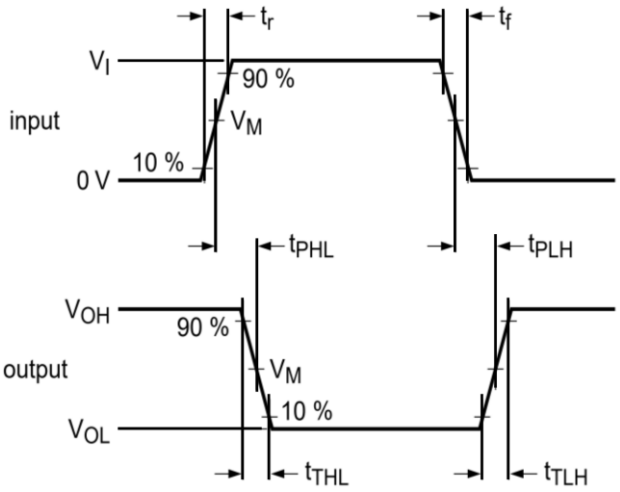


Fig. 7: Propagation delay and the output transition time of HEF4093 (NAND gate).

In accordance with different values of propagation delay for logic gate, power switches turn-on and turn-off time can be calculated. For high-side power switch (IRF5305) (Fig. 8- a):

Turn-on: t_{PLH}(NAND)+ t_{PLH}(NAND)+ t_{PLH}(AND)+ t_{on}(IRF5305) = 234 ns (2)

Turn-off: t_{PHL}(AND)+ t_{off}(IRF5305) = 94 ns (3)

For low-side power switch (IRFZ44) (Fig. 7- b):

Turn-on: t_{PLH}(NAND)+ t_{PLH}(NAND)+ t_{PHL}(OR)+ t_{on}(IRFZ44) = 192 ns (4)

Turn-off: t_{PLH}(OR)+ t_{off}(IRFZ44) = 36 ns (5)

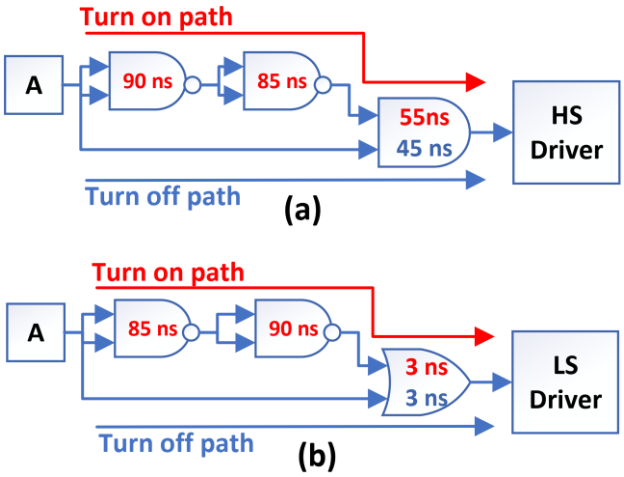


Fig. 8: High/Low side propagation delay of logic gates during turn-on or turn-off interval.

Results of calculation and simulation confirm that logic gates PD act as DT and prevent simultaneous conduction of power switches during the arrival gate drive signal (Fig. 9).

The timing diagram of logic gates proves the discrepancy between the theoretical propagation delays listed in the datasheet and practical values. As depicted in the figures, t_{PLH} and t_{PHL} are at least two orders of magnitude higher than the typical ones.

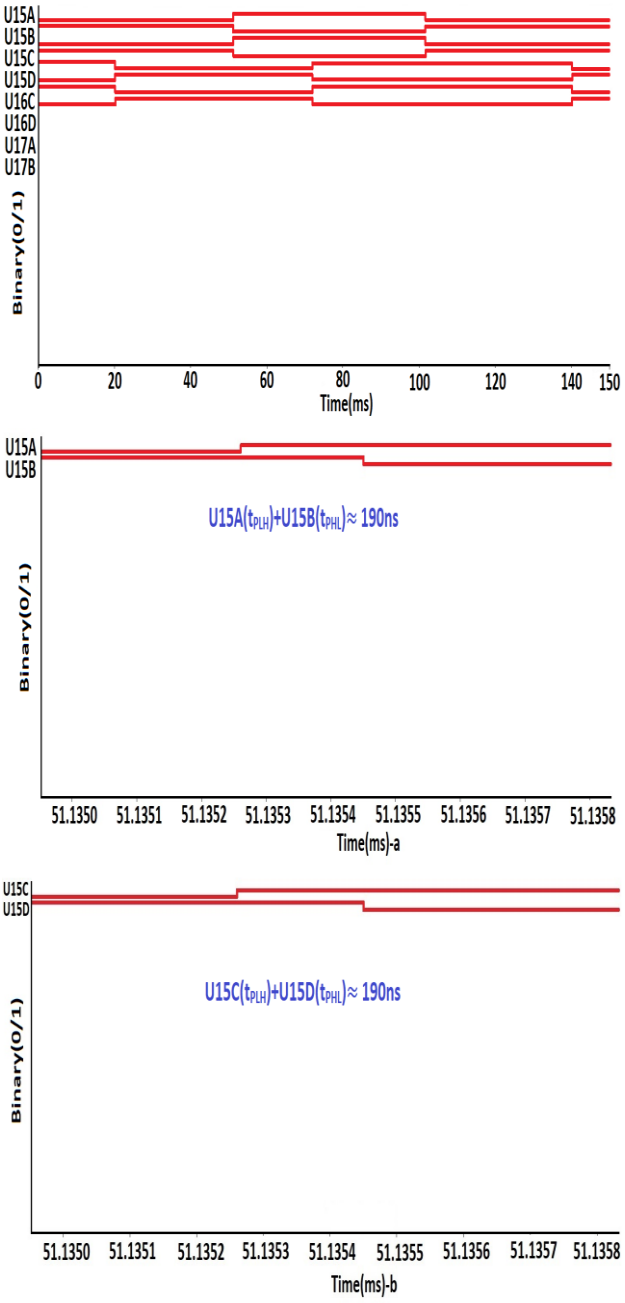
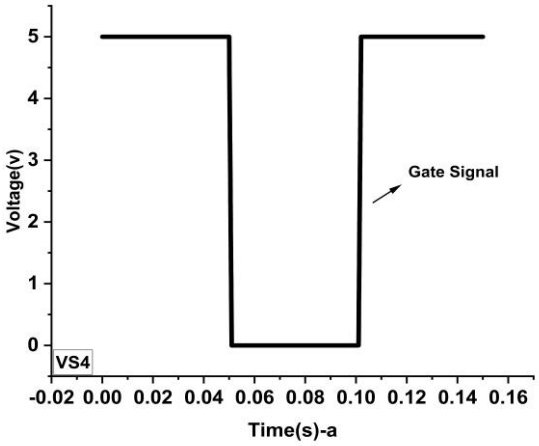
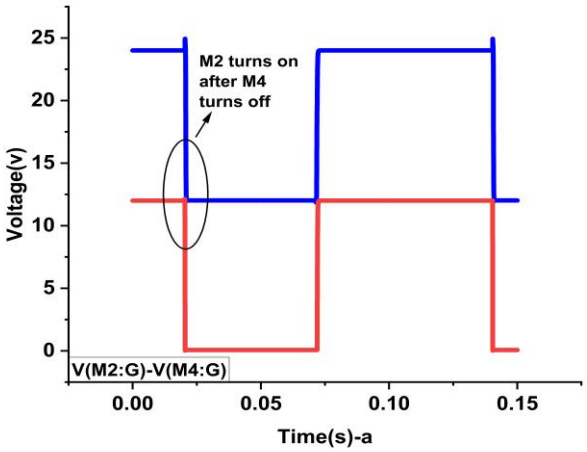
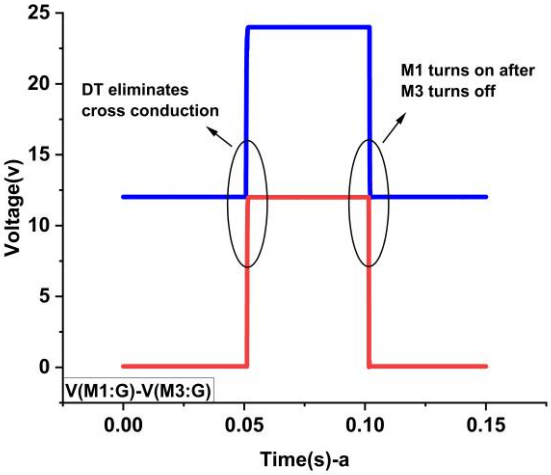


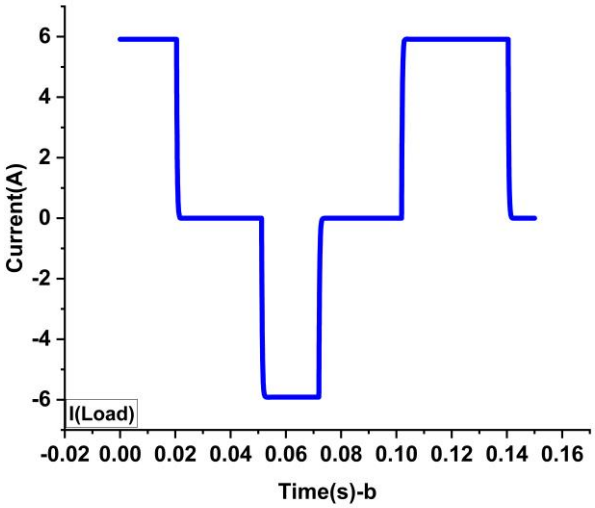
Fig. 9: Digital Timing diagram of logic gates. (a) and (b) show the propagation delay for Nand gates when different input signals impact on output (t_{PHL},t_{PLH}).

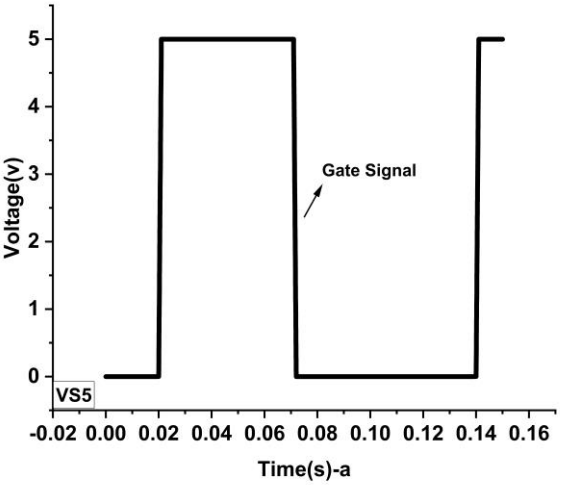
Simulation of the proposed HB driver by analyzing voltages and currents used to test the driver behavior under operating conditions that showed the validity of the schematic diagram of Fig. 5 and its method for shoot-through elimination (Fig. 10).

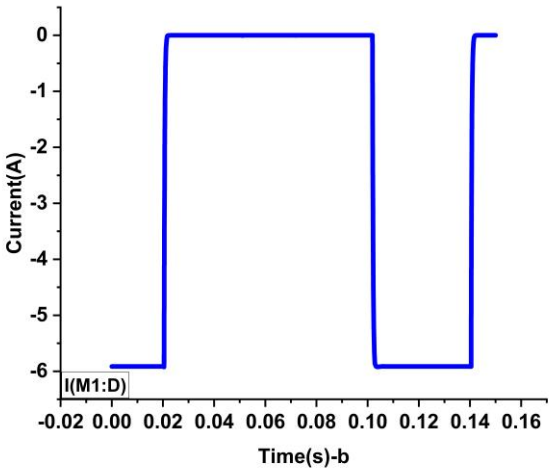

Voltage(v)
Gate Signal
VS4
Time(s)-a


M2 turns on after M4 turns off
Voltage(v)
V(M2:G)-V(M4:G)
Time(s)-a


DT eliminates cross conduction
M1 turns on after M3 turns off
Voltage(v)
V(M1:G)-V(M3:G)
Time(s)-a


Current(A)
I(Load)
Time(s)-b


Voltage(v)
Gate Signal
VS5
Time(s)-a


Current(A)
I(M1:D)
Time(s)-b

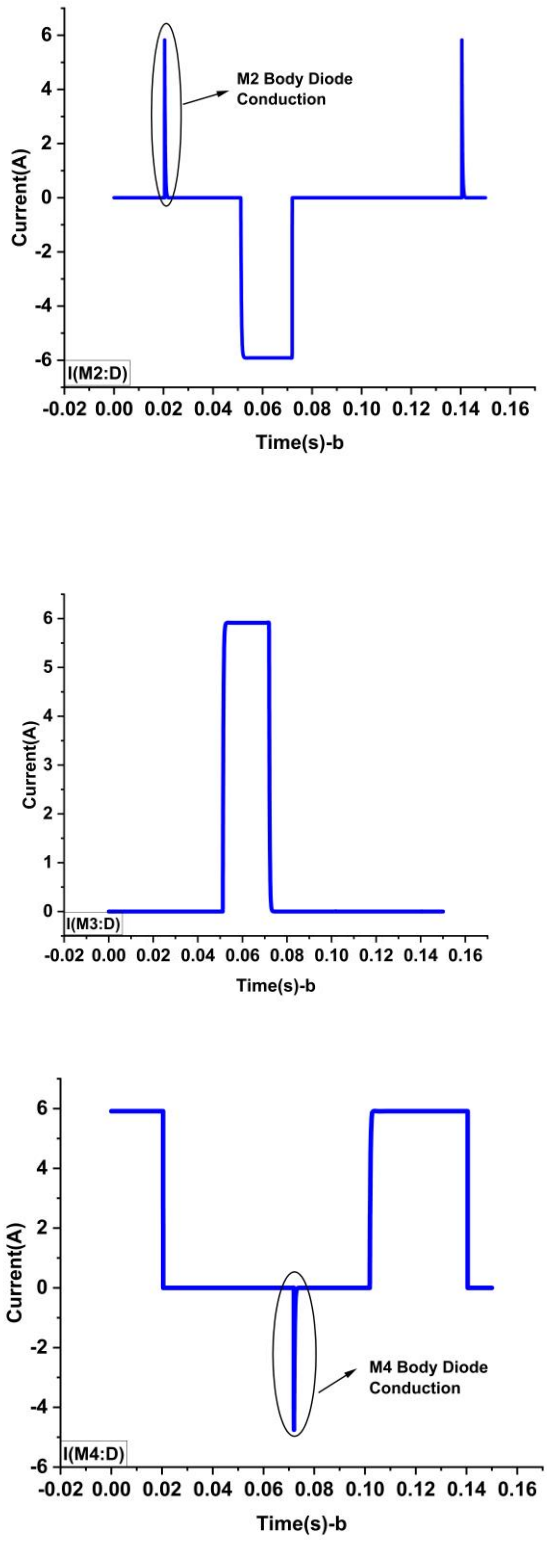


Fig. 10: voltage and current waveforms of the proposed HB driver. (a): CMOS switching voltages operation without overlapping due to the proper DT in the arrival gate drive signal; (b): load and CMOS switches currents during switching without any cross-conduction current.

Experimental results and prototype pictures of the HB driver are shown in Figs. (11-13). As expected, the proposed HB driver circuit drives the linear actuator as an inductive load without cross-conduction. Compared with other research articles [20] that fixed DT is used to overcome the cross-conduction, the method proposed in this paper is practicable and not complicated for implementing. On the other hand, most of them must use additional circuits like current polarity detection to eliminate DT effects resulting in hardware complexity and not being reliable because there is the noise and current ripple which can create a false zero crossing of the load current.

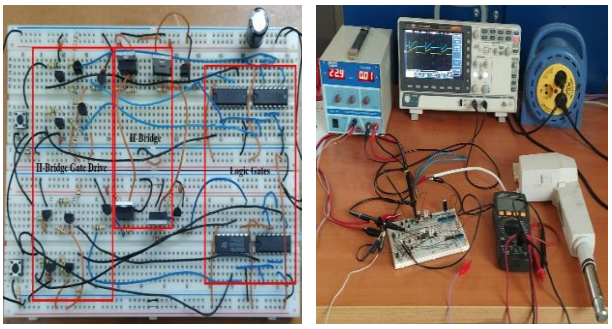


Fig. 11: prototype picture of the proposed HB driver circuit.

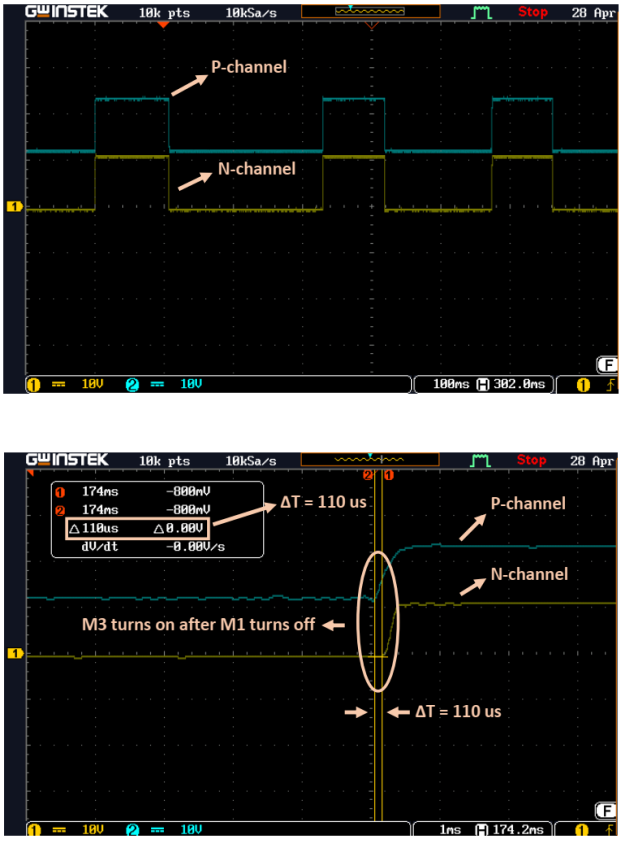


Fig. 12: Experimental results of the CMOS transistors switching while logic gates propagation delay eliminates cross-conduction without inductive load

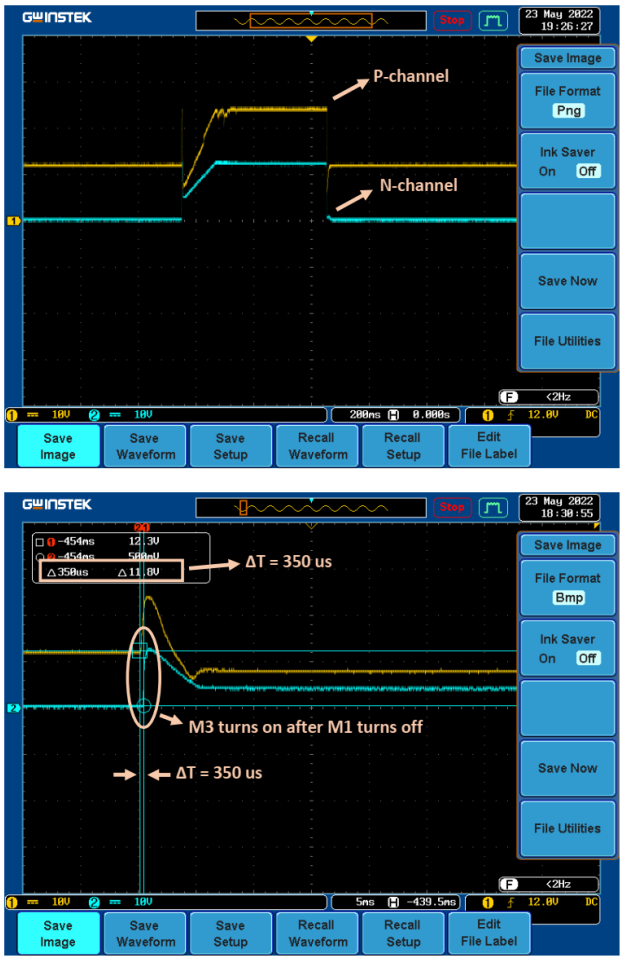


Fig. 13: Experimental results of the CMOS transistors switching while logic gates propagation delay eliminates cross-conduction with inductive load.

Conclusion

The transition delay discrepancy in MOSFET switches leads to cross-conduction in the H-bridge driver resulting in a shoot-through current. This paper investigates a novel dead-time generation method for H-bridge drivers based on CMOS transistors. As noted, dead-time should be higher than the MOSFETs turn-off time ($DT>t_{off}$) to ensure safe operation. In this paper, logic gates propagation delay included AND, NAND, and OR gates are used to generate dead-time. Dead-time value can be chosen at least two orders of magnitude higher than the turn-off time to ensure the cross-conduction elimination and the experimental results validate the accuracy of the proposed method.

Author Contributions

M. Karimi designed the experiments. M. Karimi and D. Dideban collected and carried out the data analysis. M. Karimi interpreted the results and wrote the manuscript.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

DT	Dead-Time
SH	Shoot-Through
PD	Propagation Delay
DC	Direct-Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
HS	High-Side
LS	Low-Side
t_{PLH}	LOW to HIGH propagation delay
t_{PHL}	HIGH to LOW propagation delay

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