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Research paper

Feasibility of Digital Circuit Design Based on Nanoscale Field-Effect Bipolar Junction Transistor

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Abstract

Background and Objectives: The Field-effect Bipolar Junction Transistor (FEBJT) is a device with a bipolar junction transistor (BJT) characteristics except that it is designed with standard CMOS technology. Therefore, it can be implemented in nanometer dimensions without the usual restrictions in fabricating the nanoscale BJTs. In addition to the advantages that FEBJT has as a bipolar junction transistor in analog circuits, it can also be used to design digital circuits. Here, we have investigated the capability of FEBJT as the base of a new digital family in nanometer scales.

Methods: To do this, we have designed and simulated an inverter logic gate based on FEBJT. We have presented this logic gate's static and dynamic assessment criteria and compared these characteristics with other technologies. Also, a three-stage ring oscillator circuit based on FEBJT is designed and presented. A three-dimensional TCAD Mixed-Mode simulator has been used for the simulations.

Results: The value of maximum frequency, PDP, dynamic power, and ring frequency are calculated 0.25THz, 38×10^{-17} J, 94uW, and 85GHz, respectively.

Conclusion: The excellent function of the FEBJT-based inverter gate and oscillator demonstrates that this device can be used as the base of new digital circuits and can open a doorway to the nanoscale CMOS digital family.

Introduction

The first semiconductor transistor was built in 1947. This element was called the bipolar junction transistor (BJT) developed by Schokley, Barden, and Brattain at Bell Lab [1]. The BJT has high current gain, high speed, and low input capacitance. With the advent of technology and the shrinking of electronic circuits, the fabrication of BJTs on the nanometer scale faced some restrictions. Reducing the width of the base area to nanometer dimensions was a significant obstacle to making this transistor smaller. MOS Field-Effect Transistors (MOSFETs) were another type of transistor that evolved rapidly, and CMOS technology replaced BJT in many circuits. One of the reasons for the development of CMOS technology was the possibility of manufacturing these elements in nanometer dimensions. Despite the recent advances in field-effect transistors, the specific features of bipolar transistors such as high current gain have led researchers to continue to look for solutions to utilize BJT transistors alongside MOSFETs. To this end, several papers have been presented that attempt to use both transistors at the same time or provide a solution to fabricate a smaller bipolar junction transistor to utilize the powerful features of the BJT transistor in today's small-scale digital industries [2]-[20].

By integrating BJT and CMOS transistors, BiCMOS technology simultaneously uses each of these transistors' special features [2]-[8]. The BJT transistor has been implemented horizontally, allowing for a smaller base area width. Plasma charging and polarity control of

electrodes have been proposed as other methods to avoid the need for silicon doping to create bases, collectors, and emitters in the BJT structure [9]-[17]. Another proposed device is the Field-Effect bipolar junction transistor (FEBJT), which is a BJT that is designed based on the idea of changing the doping level of the semiconductor by the electric field of the gate electrodes [18]-[20]. In other words, this device enables the implementation and fabrication of a BJT transistor with CMOS technology. In FEBJT, a BJT transistor's base, collector, and emitter regions are created using three-gate electric fields, called the gate-base, gate-collector, and gate-emitter, respectively. This structure can reduce the width of the BJT transistor to 7 nm. In addition to the analog advantages of FEBJT, this device can turn on and off with the base, emitter, and collector gates [18]-[20]. Therefore, digital electronics can be designed based on FEBJT without the current shrinking of the base electrode in BJT-based digital circuits. What this paper aims to present is to show the feasibility of digital applications for FEBJT.

In this paper, an inverter logic gate, as the base block of the digital family, is simulated and presented. The circuit design and transition characteristic diagrams are examined. The transient state responses of the segment and the times of the ups and downs have also been measured and calculated. Noise calculation at the primary logic gate is also performed and presented.

Field-effect Bipolar Junction Transistor (FEBJT)

Fig. 1 shows the schematic of FEBJT. This structure is simulated by the TCAD-3D simulator. Fig. 1(a) is the side view of this element. The design parameters are detailed in Table 1. The structure has three electrodes on the insulator: gate-collector, gate-base, and gate-emitter. It also has three common BJT electrodes: the collector, the emitter, and the base. The base electrode can be on either side of the structure. Fig. 1(b) shows the top view of the structure and the location of the base electrode. By applying a positive voltage to each gate, the n-type region can be created, and by using a negative voltage, the p-type region can be formmade on the silicon surface under the gate. Thus, it can be said that the structure is similar to MOSFET, except that the three gates are placed on the oxide instead of one gate [18], [20].

Due to the positive or negative voltage applied to the gates, there are eight modes for the silicon channel under the gates. The eight modes are shown in Table 2. Among the eight possible modes for the transistor channel, mode 3, which creates the npn structure within the channel, which is in accordance with the npn-BJT, is considered as on mode. Mode 6 of this table is considered as OFF mode [18]. Fig. 2 illustrates the circuit schematic of this device. Using this segment, two types of n-channel and p-channel can be designed according to npn and pnp BJTs. The device is designed based on SOI (Silicon on Insulator) technology. The base width of the proposed FEBJT is considered 20nm. The feature that determines FEBJT's speed and current gain is the size of the base gate, which is 20nm. The mixed-mode module of the ATLAS simulator is used for circuit model extraction. Using this module, the devices can be simulated numerically. A SPICE-like circuit description is provided in the MixedMode module. In other words, after the definition of a new concept device (like FEBJT) in the ATLAS-TCAD 3D simulator, the MixedMode module can extract the library of the new device. Different analog or digital circuits can then be defined in a SPICE-like description.

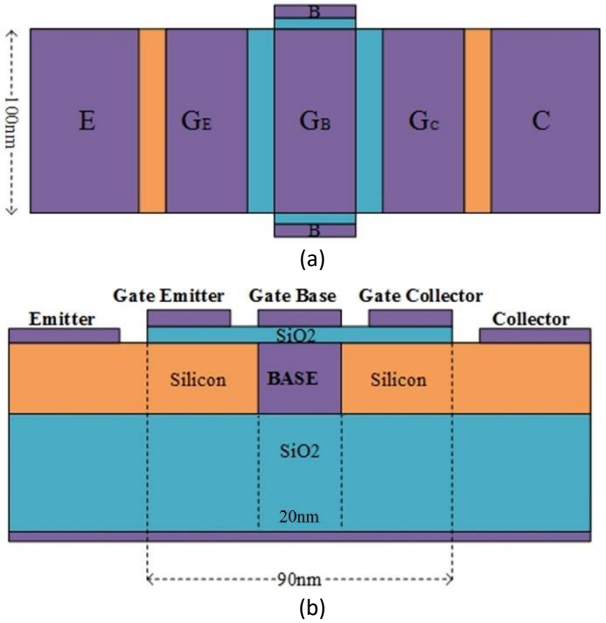

Fig. 1: (a) Side view of FEBJT. Three gates over a silicon channel induce the channel's emitter, base, and collector area. (b) Top view of the FEBJT structure. GE, GB, and GC are gate-emitter, gate-base, and gate-collector, respectively.

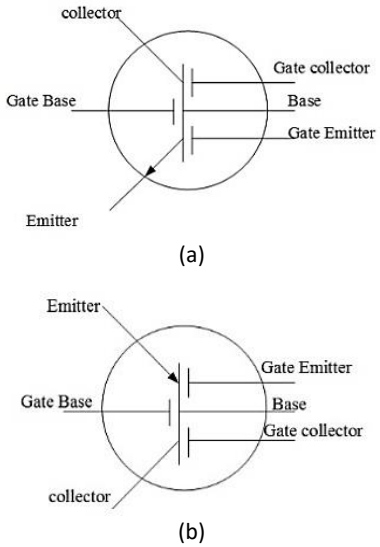

Fig. 2: (a) Circuit schematic model for npn FEBJT, (b) Circuit schematic model for pnp FEBJT.

Table 1: The design parameters of FEBJT

Symbol	Value
Thickness of Silicon film	100nm
Thickness of buried oxide	400nm
Thickness of gate oxide	5nm
Width of Structure	100nm
Length of G_E and G_C	30nm
Length of G_B	20nm
Emitter Length	40nm
Collector Length	40nm
Emitter Doping Concentration	$1\times10^{19}cm^{-3}$
Collector Doping Concentration	$1\times10^{18}\ cm^{-3}$
Channel Doping	$3\times10^{17}\ cm^{-3}$

Table 2: Possible modes for silicon channels in the FEBJT structure

STATE	Type of Structure	V_{GE}	V_{GB}	V_{GC}
1	n-nnn-n	+	+	+
2	n-nnp-n	+	+	-
3	n-npn-n	+	-	+
4	n-pnn-n	-	+	+
5	n-ppn-n	-	-	+
6	n-pnp-n	-	+	-
7	n-ppn-n	-	-	+
8	n-ppp-n	-	-	-

Inverter Logic Gate Based on FEBJT

A. Static Characteristics

Fig. 3 shows the designed inverter logic gate using FEBJT. Like CMOS inverter gate, which is designed using two complement n-channel and p-channel MOSFETs, the FEBJT inverter gate is also designed by Table 1: The structural design parameters for FEBJT. Combining two n-channel and p-channel transistors. The voltage applied to the electrodes of this structure is illustrated in Fig. 3.

Table 3 shows how to apply voltage to the device gates to generate the *low* and *high* logic outputs. Important parameters must be considered to check the quality of an inverter gate. The most important of these factors are voltage transient characteristic, output transient mode characteristic, output capacitance, output resistance, Power Delay Product (PDP), and speed [21]-[30]. The voltage transfer characteristic is a graph showing the output voltage changes relative to the input voltage. Fig. 4 shows the transient voltage characteristic of the inverter logic gate circuit with the FEBJT device. The input voltage is swept from -1 to 1 volt to obtain this characteristic. As specified in Table 3, the input voltage is applied to the gate-emitter (GE) and gate-collector (GC). Gate-base (GB) is also biased with VCC (1V).

The values are shown in Fig. 4 are used to calculate the noise margin. V_{OH} refers to the maximum output value known as logic 1. V_{OL} refers to the minimum output value known as logic 0. V_{IH} refers to the maximum input value known as logical input 1. V_{IL} refers to the minimum input value known as logical input 0. Table 4 shows the values of the parameters extracted from the voltage transient characteristic. The Noise Margin Low (NML) and Noise Margin High (NMH) values can be calculated from (1) and (2) [31]:

$$NM_L = V_{IL} - V_{OL} \quad (1)$$

$$NM_H = V_{OH} - V_{IH} \quad (2)$$

By placing the values extracted from Fig. 4 in the above equations, the NML and NMH are calculated 0.43 and 0.79 volts, respectively. It is worth noting that depending on whether the input signal is applied to the gate or base electrodes, different circuits can be designed as NOT-gate based on FEBJT. Fig. 4, the manuscript shows one possible configuration for the NOT-gate circuit in which the input is applied to the side gates of both transistors. Each designed inverter circuit would have specific voltage transfer characteristics curves (VTC), which the carrier concentrations and dopant densities can change through the channel. The reason for this change is the resistivity of the channel, which is controllable by different doping concentrations.

Fig. 5 shows the VTC for four different doping levels of the channel. To explain the reason for changing the curves shown in Fig. 4, look back at the schematic of the inverter gate in Fig. 3 inside the manuscript. As shown, there are two complementary FEBJT in a NOT-gate to create inverting behavior. Increasing the doping level of each transistor results in decreasing the channel resistivity in that transistor. By increasing the hole concentrations in pnp FEBJT, the resistivity of the above transistor decrease, and consequently, the VTC shifts to higher voltages in the right side of VTC. When the electron densities increase in npn FEBJT, the resistivity of the bottom transistor decrease and the VTC shifts to the smaller voltages and right side of the curve.

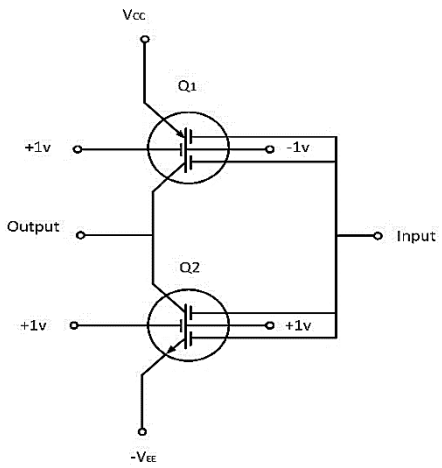

Fig. 3: The designed inverter logic circuit based on FEBJT.

Table 3: Truth table for FEBJT-based inverter logic gate

Input	Q_1	Q_2	G_E	G_C	G_B	Output
Low	on	off	input	input	Bias(+1v)	High
High	off	on	input	input	Bias(+1v)	Low

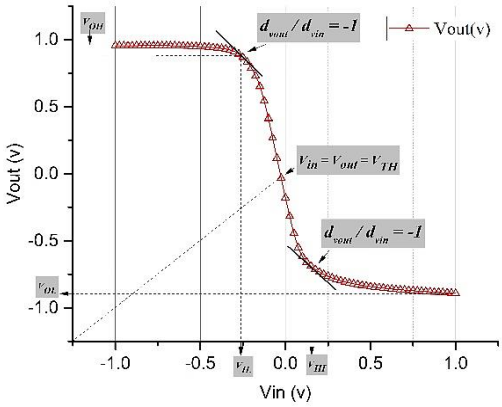

Fig. 4: The voltage transfer characteristic of the inverter logic gate circuit or not gate with the FEBJT device.

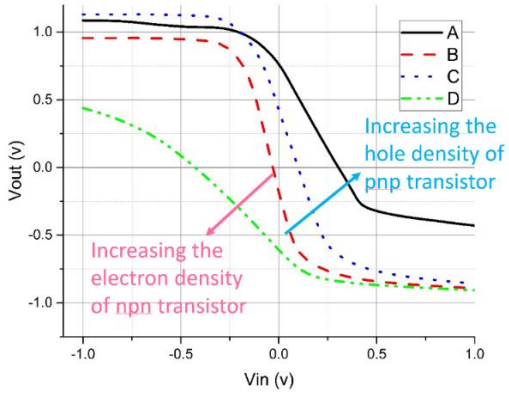

Fig. 5: The VTC for four different doping levels of the channel. By increasing the hole concentrations in pnp FEBJT in NOT-gate, the resistivity of the above transistor decreases. Consequently, the VTC shifts to higher voltages in the right side of VTC. When the electron densities increase in npn FEBJT, the resistivity of the bottom transistor decrease and the VTC shifts to the smaller voltages and right side of the curve.

B. Dynamic Characteristics

Fig. 6 shows the transient response of the inverter circuit based on FEBJT. As is demonstrated in Fig. 6(a), a voltage pulse in the range of (-1V to 1V) with a period of 2 microsecond is applied as the input signal. The output signal is also demonstrated in this figure. As can be seen, the output signal exactly follows the input in reverse. To characterize the dynamic performance of a logic-circuit family, the propagation delay of the basic inverter gate is usually examined [31].

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Table 4: The value of voltage transfer characteristic parameters

Voltage	Amount (v)
V_{OH}	0.95
V_{OL}	-0.88
V_{IL}	-0.27
V_{IH}	0.16
V_{TH}	-0.04

The inverter propagation delay time (τ_p) is defined as the average of the high to low and low to high propagation delays as follows [31]:

$$\tau_p = \frac{\tau_{phl}+\tau_{plh}}{2} \quad (3)$$

In this equation, τ_{phl} and τ_{plh} are defined as the required time for the output to reach 50% of the rail-to-rail voltage. Two other parameters to examine the dynamic performance of digital circuits are the rise and the fall time of the output pulse. These two parameters (τ_r) and (τ_f) are defined as the required time for the output to change from 10% to 90% and from 90% to 10% of the rail-to-rail voltage, respectively. The transient responses are zoomed-in Figs. 6(c) and 6(d). The calculated dynamic parameters for the FEBJT inverter are listed in Table 5.

We have measured the output of the proposed inverter gate for four different load capacitors. The propagation delay times decrease when the output capacitor decrease. The rise, fall, and propagation delay times are shown in Fig. 7 as a function of the load capacitor. This curve shows that the parasitic capacitor at the output node is around 500fF. One of a digital circuit's most important design parameters is the Power Delay Product (PDP). This parameter indicates the amount of energy needed to change the output from the maximum value to its minimum value and vice versa. PDP can be calculated from the following equation [31]:

$$PDP = C_{load} \times {V_{dd}}^2 \quad (4)$$

C_{load} is the load capacitance that indicates the output node capacitance, and V_{dd} is the power supply voltage. There are different solutions for estimating the output node capacitance [31]. Here, we first put an external 1pf capacitor at the output node to calculate the output resistance from the time constant of the output curve (see Fig. 6(b)). After determining the output resistance, we looked back to the output curve of the inverter when no external capacitance was connected (see Fig. 6(a)). By knowing the value of the output resistance (25kΩ), the output node capacitance (C_{load}) was calculated 0.06 fF from the time constant of the output curve. Using (4), PDP was calculated about 38×10^{-17} J. Dynamic power, and the maximum frequency of the inverter logic gate are the

other important dynamic parameters that estimate the performance of a new digital family [24]. Using (5) and (6) [31], the maximum frequency and the dynamic power of the FEBJT inverter gate were calculated 0.25THz and 94uW, respectively.

$$F_{max} = \frac{1}{(\tau_{phl} + \tau_{plh})} \quad (5)$$

$$P_D = C_{load} \times {V_{dd}}^2 \times F_{max} \quad (6)$$

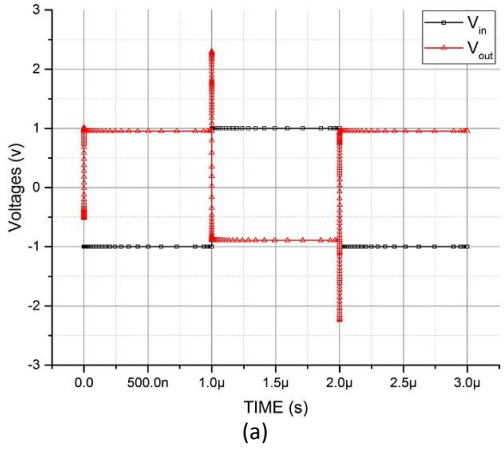
The important digital factors of the FEBJT inverter are compared with other field-effect transistors with an almost similar gate length in Table 6.

C. Ring Oscillator

In this part, a three-stage ring oscillator based on FEBJT is designed and simulated, and its performance is evaluated and compared with other technologies. Fig. 8(a) demonstrates the designed ring circuit based on FEBJT. This oscillator is a combination of an odd number of inverters, and the output of each stage is given as input to the next stage. The output of the last stage is connected to the first stage, thus forming a ring. Each inverter stage provides a specific delay time; thus, the three-stage circuit starts to oscillate at a particular frequency [30]. The oscillation frequency is the function of the delay time of each stage and the number of stages used in the ring circuit [30]:

$$F_{osc} = \frac{1}{2n\tau_p} \quad (7)$$

N is the number of the stages, and τ_p is the delay time of a single inverter stage. Considering n=3 and τ_p=2.01p, the oscillation frequency of the designed ring is calculated 85GHz. The output voltage of the ring oscillator based on FEBJT is demonstrated in Fig. 8(b). The performance of the designed ring oscillator is compared with other technologies in the almost similar gate length in Table 7. As can be seen in this table, the operation frequency of the ring oscillator based on FEBJT is larger than the other comparable proposed devices in many published works, and that's while the dynamic power of the inverter stage is smaller than the others.



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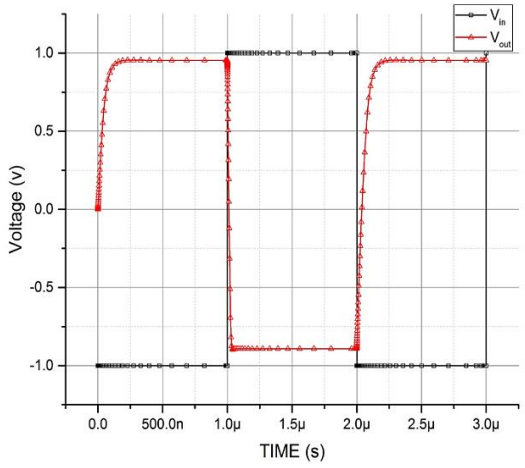

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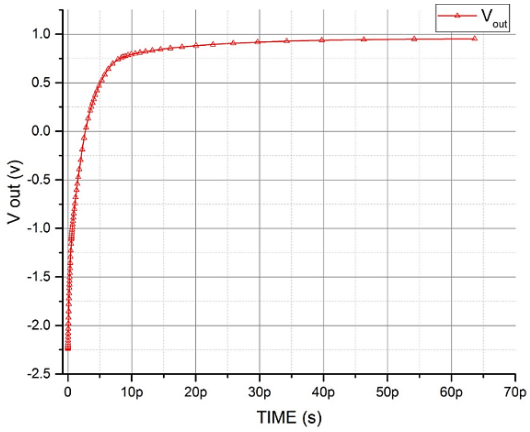

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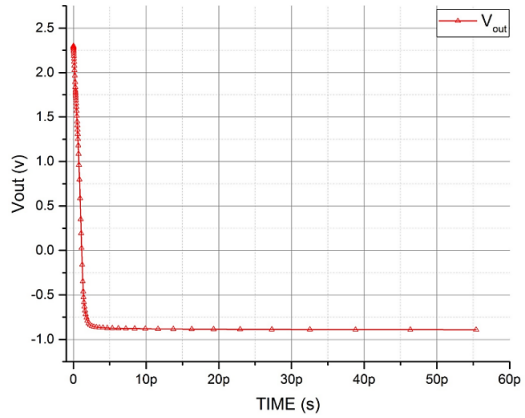


(d)

Fig. 6: The transient response of the inverter circuit based on FEBJT. (a) without the external capacitor, (b) with 1pf external capacitor. (c) The rise up of the output voltage is zoomed, τ_r is measured 7.79 ps. (d) The fall down of the output voltage is zoomed, τ_f is measured 0.84 ps.

Results and Discussion

The static and dynamic simulation results for the inverter logic gate based on FEBJT and the calculated performance of the ring oscillator built with FEBJT demonstrate the ability to use FEBJT in the design of digital circuits.

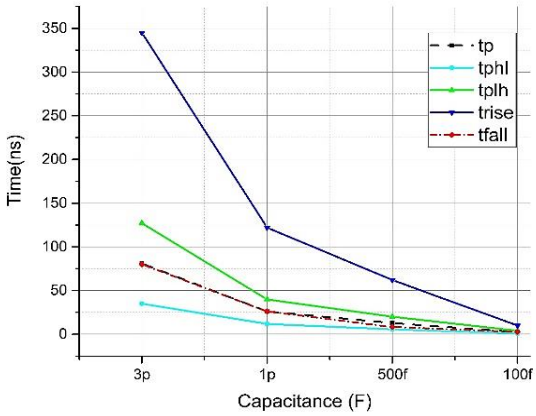


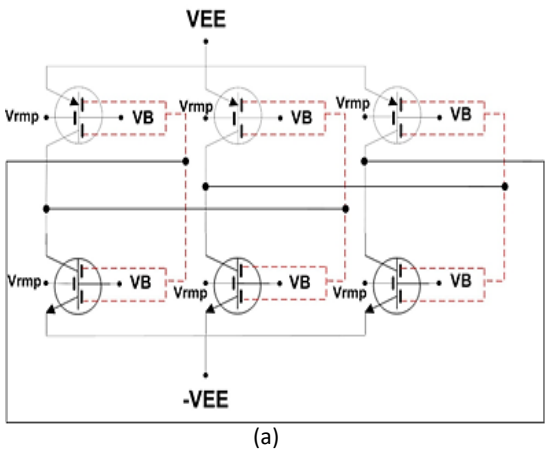
Fig. 7: The output of the proposed inverter gate for four different load capacitors. The rise, fall, and propagation delay time as capacitor function. As can be seen, the propagation delay times decrease when the output capacitor decrease.

Table 5: The value of transient state parameters

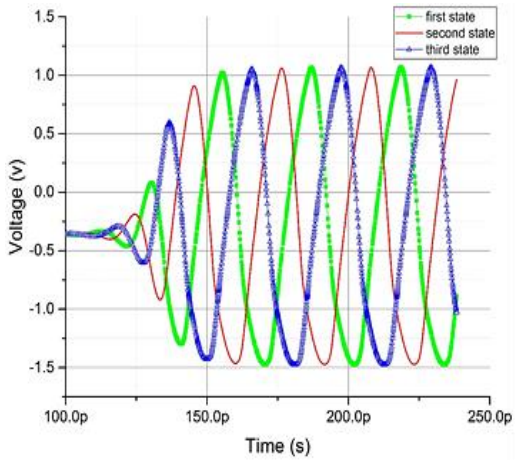
Time	Amount (s)
t_{phl}	1.11p
t_{plh}	2.89p
t_{fall}	0.84p
t_{rise}	7.79p
t_p	2.01p

Table 6: Comparison of the Field-effectBJT Reverse Logic Gate with other devices [29], [32]-[36]

Device	Structure	T_p (ps)	PDP (j)	Gate Length (nm)
This work	Field-effectBJT	2.01	38×10^{-17}	20
[29]	S-FED	1.04	6.2×10^{-18}	25
[32]	FINFET	8	7.0×10^{-18}	20
[33]	S-bulk Finfet	53000	3.0×10^{-13}	17
[34]	HTFET	710	3.6×10^{-20}	20
[35]	FINFET	2.3	0.01×10^{-21}	16-32
[36]	CNTFET	24	0.04×10^{-18}	20



(a)



(b)

Fig. 8: (a) The designed three-stage ring oscillator circuit based on FEBJT. (b) The oscillation of the three-stage circuit shown in Fig. 6(a). The oscillation frequency is measured 84GHz.

Table 7: The performance of the designed ring oscillator is compared with other technologies [37]-[47]

Device	Structure	State of ring	Frequency (GHz)	$Power_{dyn}$ (w)	Gate length(nm)
This work	FEBJJT	3	82	94×10^{-6}	20
[37]	DJ-JNT	3	4	-	20
[38]	FDSOI	3	2.45	-	32
[39]	Dg-JNT	3	52	-	20
[40]	CMOS	4	8.33	435×10^{-6}	65
[41]	FDSOI	3	49	3.77×10^{-3}	28
[42]	CMOS	4	16	46.2×10^{-3}	20
[43]	FINFET	3	40	-	20
[44]	V-TFET	11	0.6	86×10^{-9}	20
[45]	DG-FET	3	4.14	12×10^{-6}	20
[46]	TFET	9	-	1.5×10^{-15}	14
[47]	NCFET	17	2.9	-	18

Conclusion

A digital circuit was designed using the FEBJT element. This circuit is an inverter logic gate. Important features and values calculated, such as voltage transient characteristic, transient state, output capacitance, output resistance, and PDP, indicate that FEBJT is applicable for digital applications. Further, it is recommended to research other digital basic circuits with the help of this device with unique features.

Author Contributions

M. Amirmazlaghani designed the experiments. A. Shokri performed the simulations. M. Amirmazlaghani and A. Shokri interpreted the results and wrote the manuscript.

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Conflict of Interest

The author declares that there is no conflict of interests regarding the publication of this manuscript.

Abbreviations

FEBJT	Field-effect Bipolar junction transistor
BJT	bipolar junction transistor
PDP	Power Delay Product
CMOS	Complementary Metal Oxide Semiconductor
FET	Field-effectTransistor
MOSFET	Metal Oxide Semiconductor Field-effectTransistor
NML	Noise Margin Low
NMH	Noise Margin High

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