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Research paper

CNN-Based Placement and Multi-Objective Routing for Analog Circuits with Simulated Annealing and NSGA-III

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Abstract

Background and Objectives This research aims to optimize component placement in integrated systems using evolutionary algorithms. The primary goal is to generate a compact floorplan while satisfying design constraints, particularly in analog circuits where symmetry and proximity constraints are critical to minimizing coupling interference and enhancing performance. The study proposes using a convolutional neural network (CNN) to extract these placement constraints, with its parameters optimized via the non-dominated sorting genetic algorithm III (NSGA-III). Additionally, a hybrid routing approach combining simulated annealing (SA) and NSGA-III is introduced to improve routing efficiency through multi-objective optimization.

Methods: The placement constraints, including symmetry and proximity requirements, are extracted using a CNN, whose parameters are optimized by NSGA-III. For routing, a hybrid approach is employed where SA generates initial routing solutions, which are then refined by NSGA-III for multi-objective optimization. The proposed method is implemented on a two-stage recycling folded cascade (RFC) amplifier in 0.18µm CMOS technology with a 1.8V supply voltage. A dedicated MATLAB toolbox is developed to facilitate placement while adhering to design rules using optimization algorithms.

Results: Simulation results confirm the effectiveness of the proposed methodology, demonstrating optimized placement and routing with improved circuit performance. The combination of CNN and NSGA-III successfully generates a compact and efficient layout, while the hybrid routing approach (SA + NSGA-III) enhances the routing process. The RFC amplifier case study shows better utilization of physical resources and performance improvements, validating the method's efficiency.

Conclusion: This study demonstrates that the proposed method, integrating evolutionary algorithms and CNN, effectively optimizes placement and routing in integrated systems. The CNN-based constraint extraction and NSGA-III optimization enable compact layouts, while the hybrid routing approach improves multi-objective optimization. Simulations on the RFC amplifier confirm enhanced circuit performance and resource utilization. This method offers significant advantages over traditional approaches and is applicable to complex and industrial designs.

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Introduction

After some time, a designer becomes accustomed to the design rules specific to a given process, including the dimensions and spacing associated with it [1]-[3]. As integrated circuit manufacturing technology continuously advances and becomes more sophisticated, the designer is eventually compelled (or prefers) to design and create circuits using a more advanced process. With the transition to a more advanced manufacturing process, both the dimensions and the minimum definable features shrink. Consequently, the designer must relearn all the measurements for the new process. To avoid this, one common approach for expressing design rules and measurements in manufacturing processes is the parametric method. In this approach, a parameter called lambda (λ) is introduced as a reference, with all measurements expressed in terms of this parameter. Such design rules are referred to as lambda-based rules [4]-[8]. In such cases, once the placement is fully designed, the lambda value is used to convert all dimensions from parametric to real dimensions. As mentioned earlier, for any numerical process, it is introduced as the refinement of the construction or the minimum definable dimensions. The lambda parameter for each process is typically a value approximately half of the fineness of that process. In this way, the smallest dimension that the designer can use in their placement is 2λ.

Asymmetries in all differential circuits inevitably lead to the creation of an offset with respect to the input, which can significantly affect the performance of the circuit. These asymmetries can arise due to various factors, including the physical properties of the components, their layout, and the fabrication process. While some mismatch between components is unavoidable due to inherent limitations in manufacturing, the magnitude of this mismatch can be minimized with careful attention to the symmetry of the layout. If symmetry is not adequately considered during the placement design, it can result in large offsets that degrade the accuracy and stability of the differential circuit. These offsets can cause the circuit to deviate from its expected behavior, resulting in errors, instability, and reduced overall performance [9]-[13].

One of the key areas where asymmetry arises is in the placement and orientation of transistors. When transistors are oriented differently, they can exhibit mismatched electrical characteristics, even if they are nominally identical. This mismatch can occur due to variations in the process or the geometry of the transistors, as well as differences in how they interact with the surrounding components. As a result, the overall performance of the circuit can be compromised, especially when precise symmetry is required for optimal function.

To mitigate these challenges, it is critical to implement precise symmetry constraints throughout the placement design stage. This means ensuring that the layout of the circuit is carefully balanced and that the transistors are placed in a way that minimizes mismatches. One specific issue that arises is the mismatch between transistors with different orientations [9]-[13], which can cause variations in the electrical characteristics of the transistors, such as threshold voltage, current drive capability, and other parameters. These mismatches can have a significant impact on the overall performance of the differential circuit, particularly in high-precision applications where even small offsets can lead to substantial errors.

Therefore, careful attention to symmetry, especially in the placement of transistors and other critical components, is essential to minimize these mismatches and ensure the differential circuit performs as intended. In some cases, advanced techniques such as layout optimization or the use of symmetry-enforcing design rules can help mitigate the effects of asymmetry, resulting in more accurate and stable circuits.

Routing complexity in ICs is one of the fundamental challenges in designing these circuits. In the routing process, the goal is to optimally establish connections between the various components of the circuit, making efficient use of the limited space available to the designer. With the increasing transistor density and greater circuit complexity, the number of connections and paths that must be created also increases exponentially. This turns routing into a time-consuming and challenging process that requires high precision. Additionally, electromagnetic interference, thermal issues, and power limitations are other challenges designers face during routing [14]-[18].

To address these challenges, automated methods for routing have been developed to help designers perform this process more quickly and efficiently. One such automated routing method involves the use of artificial intelligence algorithms, such as genetic algorithms or random search algorithms, which can automatically find optimal paths. These algorithms optimize routing based on criteria such as minimum distance, energy consumption, and interference avoidance. Furthermore, methods based on neural networks are also used as tools to predict complex routing behaviors. These methods can automatically perform routing tasks and minimize the designer's manual intervention, increasing design speed and reducing human errors.

The structure of the paper is as follows. In the next Section, the existing methods in the field of IC design and circuit routing are thoroughly reviewed. A novel method for placement based on a convolutional neural

network (CNN) is introduced and explained later. Additionally, the routing algorithm based on simulated annealing (SA) and non-dominated sorting genetic algorithm III (NSGA-III) is also presented and discussed. Then, in the next Section, the simulation process conducted using various tools and the analysis of the results obtained from it will be presented. Finally, the key findings of the research presented will be summarized.

Related Works

Long and his colleagues [19] emphasized the importance of considering charge (signal) in the design process. They first extracted the current (signal) paths of an analog integrated circuit (IC) and then placed MOS transistors in each current path with a predetermined direct current path from left to right. To minimize the total area of such placement, the flow paths should have uniform height, and the physical length of the flow paths should be approximately equal. When MOS devices are placed with fixed physical dimensions (i.e., a fixed number of fingers), such that the drain-source capacitance is minimized according to the current path constraints, the placement generated by the method [19] is no longer optimal. The global placement and routing problem in analog integrated circuits cannot be considered separately, as they often lead to complex constraints. In reference [20], a technique for global and partial placement is presented. During the global placement phase, a genetic algorithm is employed. In the partial placement stage, placement is based on very fast simulated annealing, and general routing is carried out using the Steiner minimum tree approach. This method allows for the optimal solution to be found by searching within a smaller area.

Current density and flux are crucial factors in positioning and routing during analog placement synthesis [21]. Current limitations are applied to sensitive nodes with uniform current or signal paths to minimize interference effects. Current density constraints are typically used for nodes with variable wire widths to prevent issues such as IR loss and electrical migration. In this article, the limitations of both charge current and current density are simultaneously considered, allowing for routing and placement with minimal area, number of arcs, interfaces, and coupling noise. Initially, an improved B* algorithm is introduced to model both the modules and intermediate connections simultaneously. Following that, a combined placement and routing algorithm is presented, which generates a placement while considering current density and charge limitations, aiming to reduce placement area, wire length, number of arcs, connectors, and coupling noise.

In [22], a tool for generating digital circuit layouts from truth tables or Boolean equations is presented. This tool employs the maze algorithm for routing in two layers. It is compatible with integrated circuit design environments such as Mentor Graphics and Cadence. The placement process in this method is straightforward, with a distance equal to the dimensions of a transistor considered between the cells. In [23], a method for designing analog and mixed circuits is presented. In this method, the maze algorithm is used for routing. One of the advantages of this approach is that it can satisfy the matching constraint between components and intermediate connection wires during routing.

The particle swarm optimization algorithm has been used for placement in FPGA circuits [24]. In the placement stage, locations are assigned to each configurable logic block (CLB) to optimize specific objectives. These objectives may include the wire length used, routing capability between blocks, and placement time. Using the first objective function, the goal is to place logic elements close to each other to minimize the wire length. The second objective function controls the amount of wire used between blocks, while the third objective function minimizes the placement time.

Proposed Method

Evolutionary algorithms are a set of stochastic search methods inspired by natural evolutionary processes in biology. These algorithms are used to solve optimization problems that are complex or difficult to address using conventional analytical methods. Instead of searching for a single solution, these algorithms perform parallel searches across a population of possible solutions. The evolutionary process involves selection, crossover, and mutation to generate new generations of solutions, gradually converging toward the optimal solution. Evolutionary algorithms are particularly useful in problems with vast, nonlinear search spaces where analytical solutions are challenging to obtain, offering the ability to find optimal or near-optimal solutions.

In 1975, Professor John Holland proposed the Genetic Algorithm (GA), and some of his students, including David Goldberg, developed it [25]-[27] A genetic algorithm is a branch of evolutionary algorithms and is based on the structure of genes and chromosomes. The working range of the genetic algorithm is very wide, and every day, with the increasing progress of science and technology, the use of this method in optimization and solving problems has been expanded. Here, the proposed placement method based on CNN and NSGA-III will be presented. Then, the routing based on SA-NSGA-III will be presented.

CNN-based Placement

The proposed placement method is based on CNN, which automatically extracts placement constraints such

as symmetry and proximity. CNNs are highly efficient in handling complex placement tasks, where these constraints play a crucial role in ensuring the correct positioning of circuit elements. The ability of CNNs to learn patterns from large datasets allows them to model the intricate relationships between components in analog circuits, facilitating optimal placement while considering both functional and physical constraints. The automatic extraction of such constraints helps streamline the design process, improving efficiency and accuracy in the overall layout.

However, determining the optimal parameters for CNN, such as filter size and the number of filters, is a challenging task. To overcome this difficulty, the optimization of these parameters is performed using the NSGA-III. NSGA-III, a multi-objective optimization algorithm, is well-suited to explore the vast search space of CNN parameters. By leveraging NSGA-III, the method can efficiently find a balance between competing objectives, such as minimizing the area, ensuring symmetry, and maintaining the desired placement constraints. This combination of CNN and NSGA-III ensures that the placement process is not only automated but also optimized for the specific requirements of the analog circuit design.

The objective functions for the NSGA-III algorithm include inference time and accuracy. These objective functions are specifically used to optimize the performance of the circuit design model. Inference time refers to the amount of time required for the model to process inputs and generate outputs, and minimizing this time can lead to faster performance in hardware systems. On the other hand, accuracy refers to the model's ability to predict correct results, and improving accuracy can contribute to more optimal and precise circuit design. By using these objective functions in NSGA-III, an optimal balance between processing speed and model accuracy can be achieved, which is crucial for designing complex and efficient circuits. The architecture of the CNN-NSGA3 is shown in Fig. 1.

For network training, we assembled an image-based dataset of analog circuit layouts that includes fundamental building blocks such as differential pairs, current mirrors, and other common analog structures. Symmetry and proximity constraints are explicitly respected when preparing the examples so that the network would learn constraint-preserving patterns. The data are collected from diverse sources (see [28]–[32]) and, after curation, the dataset comprises approximately 450 images, chosen to cover a wide variety of circuit topologies and block geometries.

All samples use an image-based layout representation (no graph-based representations were employed in this study). Every image was preprocessed to ensure a uniform input format: images were resized to the fixed spatial dimensions required by the network's image input layer. In addition to resizing, standard image preprocessing routines (such as consistent pixel scaling and ensuring consistent channel format) were applied to guarantee numerical stability and reproducibility during training.

Training is performed using stochastic gradient descent with momentum (SGDM). Key training choices made to promote stable convergence and to reduce overfitting include a conservative initial learning rate (0.001), training for up to 100 epochs with data shuffling at each epoch, and continuous monitoring of a held-out validation set. A dedicated validation datastore is used to evaluate model performance after each epoch; these validation metrics guided model selection and the stopping decision. Training progress (loss and validation curves) is monitored throughout to ensure proper convergence and to detect any onset of overfitting.

The main steps of the proposed method are as follows:

1- The network architecture should be explicitly defined. In this case, the architecture consists of a sequence of layers, including convolution2dLayer, batchNormalizationLayer, reluLayer, maxPooling1dLayer, fullyConnectedLayer, softmaxLayer, and classificationLayer. Each of these layers plays a crucial role in the network's ability to process and classify input data effectively.

2- The convolution2dLayer is influenced by several key parameters, such as filterSize and numFilters. These parameters control the size of the filters applied to the input data and the number of filters used in the convolution operation. In the proposed method, the values for filterSize and numFilters are determined in a manner that aims to achieve a balance between maximizing the model's accuracy and minimizing its inference time, ensuring that the network performs efficiently without sacrificing performance.

3- The optimal solutions for filterSize and numFilters are determined using the NSGA-III algorithm. This multi-objective optimization technique evaluates the trade-off between multiple objectives, allowing for the identification of the best combination of parameters that leads to the most effective model configuration.

4- Both the accuracy of the Convolutional Neural Network (CNN) and the inference time are evaluated by NSGA-III as part of the optimization process. The algorithm works iteratively to refine the parameters, ensuring that the final model provides the highest accuracy while maintaining a low inference time, which is crucial for real-time applications.

5- The stopping criterion for NSGA-III is the attainment of the maximum number of allowed

iterations. If this condition is not met, the algorithm continues to generate new solutions and refine its search for optimal parameters. This iterative process ensures that the solution converges to the best possible result within the given computational constraints.

6- Once the optimal parameters for filterSize and numFilters are determined, the generated solutions are passed to the routing stage. This stage involves the final steps of network design, where the appropriate routing for the circuit or system is determined based on the optimized CNN architecture, ensuring that the model's implementation is both efficient and effective in terms of hardware requirements.

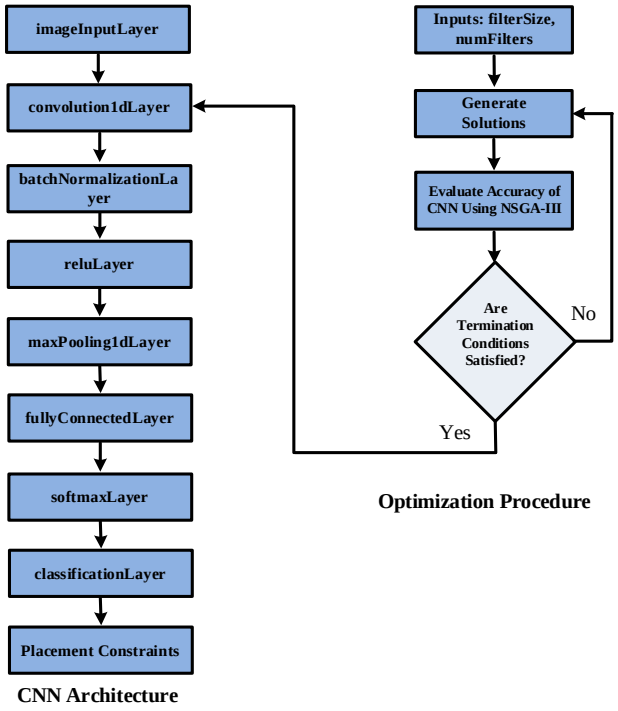


Fig. 1: CNN-based placement.

Hybrid Routing Method

In the routing stage of IC design, employing a hybrid approach that combines SA and NSGA-III can be an efficient method for finding optimal solutions. This combination leverages the strengths of both techniques to achieve high-quality routing solutions. The proposed Hybrid Approach can be described as follows:

1. Initial Solution Generation by SA
   - The SA algorithm is first used to generate an initial set of routing paths.
   - SA's capability to escape local optima ensures a diverse set of solutions, which is essential for complex routing problems.
   - The algorithm follows a cooling schedule, gradually refining solutions as it lowers the temperature, allowing it to transition from an exploratory phase to a fine-tuning phase.
   - By controlling the probability of accepting worse solutions at higher temperatures, SA prevents premature convergence and explores the solution space effectively.
2. Multi-Objective Optimization with NSGA-III
   - The best solutions obtained from SA are used as the initial population for the NSGA-III.
   - NSGA-III, a multi-objective evolutionary algorithm, improves the solutions further by optimizing multiple conflicting criteria such as power consumption, DC-gain, and Area.
   - Unlike its predecessor NSGA-II, NSGA-III employs reference point-based sorting, which enhances its performance in high-dimensional objective spaces, making it highly suitable for complex VLSI routing problems.
   - The algorithm ensures that solutions remain well-distributed along the Pareto optimal front (POF), leading to an optimal trade-off among various performance metrics.

Key advantages of this approach compared to [28] is as follows:

- Diverse Solution Generation: SA introduces diversity in initial routing paths. Global Optimality: The combination prevents premature convergence and ensures near-global optimality.
- Multi-Criteria Optimization: The approach simultaneously minimizes target specifications such as power consumption, DC-gain, and Area.
- Scalability: Suitable for large-scale VLSI designs, including Global Routing and Detailed Routing.
- Flexibility: Can be extended to optimize 3D IC routing and multi-layer interconnects.

The main steps of the proposed method, which is a hybrid approach combining SA and NSGA-III, can be described step by step as follows (Fig. 2):

- The SA algorithm is used to generate an initial set of routing solutions. This set consists of solutions that are produced based on initial criteria.
- In this step, the initial conditions (such as temperature, cooling rate, and stopping time) for the SA algorithm are configured. These parameters directly influence the quality of the initial set of solutions.
- The SA algorithm is applied iteratively on different sets of solutions to reach a set of solutions that are optimal or near-optimal.
- After the initial set of solutions is generated

by SA, this set is passed to the NSGA-III algorithm for multi-objective optimization.

- In this step, NSGA-III optimizes the solution set using various sorting and selection techniques for multi-objective optimization, considering different objectives (such as minimizing wire length, number of vias and number of bends).
- After multi-objective optimization with NSGA-III, a set of solutions is evaluated based on their performance with respect to different objectives, and the best solutions are selected to be introduced as the final solution.
- In the next stage, post-layout simulation is performed to validate the functionality and performance of the optimized design under more realistic conditions, including parasitic effects. Based on this step, the final layout is generated, which ensures that the proposed design not only satisfies theoretical optimization criteria but also meets practical implementation requirements.

Simulation Results

Automatic placement and routing of analog circuits have been performed in 0.18 µm CMOS technology with a supply voltage of 1.8 V. For this purpose, a dedicated toolbox has been developed using MATLAB software, incorporating advanced algorithms to optimize the placement and routing of analog circuits efficiently. The software used is MATLAB R2013a. System specifications used are core™ i5-4460 CPU @ 3.2 GHz with 16 GB of memory. The input images used for training the network were collected from various sources, including [28]. The parameters of the genetic algorithm in the placement stage are as follows:

- Maximum number of iterations = 20
- Population size (nPop) = 100
- Crossover percentage (pCrossover) = 0.5
- Mutation percentage (pMutation) = 0.5
- Mutation rate = 0.3

The number of parents is calculated from the following relationship:

$$2*\text{round}(\text{pCrossover}*\text{nPop}/2) \quad (1)$$

The number of mutants is calculated from the following equation:

$$\text{round}(\text{pMutation}*\text{nPop}) \quad (2)$$

Mutation step size is calculated from the following equation:

$$0.1*(\text{VarMax}-\text{VarMin}) \quad (3)$$

where VarMin and VarMin are the lower and upper limits of the variables, respectively. These parameters are chosen in such a way that there is a compromise between the speed and accuracy of the algorithm.

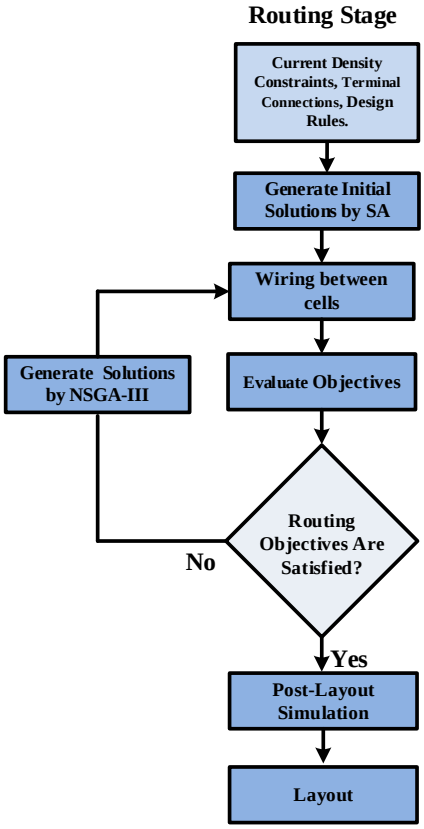


Fig. 2: Hybrid routing method.

The schematic of the two-stage recycling folded cascade (RFC) amplifier is shown in Fig. 3 [29]. By leveraging the multi-path scheme and enhancing the effective transconductance, the overall performance of the operational transconductance amplifier (OTA) is significantly improved. This approach leads to a substantial increase in the OTA's DC gain, which is crucial for achieving higher accuracy and better signal integrity in analog and mixed-signal circuits [30]-[31]. The dimensions of the amplifier are reported in Table 1. The detailed dimensions of the amplifier, including transistor sizes and passive component values are presented in Table 1.

As highlighted in the proposed method, a CNN has been employed to automatically extract symmetry and proximity constraints, which play a crucial role in optimizing the placement and routing of analog circuits. By leveraging deep learning techniques, the CNN efficiently identifies and enforces these constraints, reducing design complexity and improving overall circuit performance.

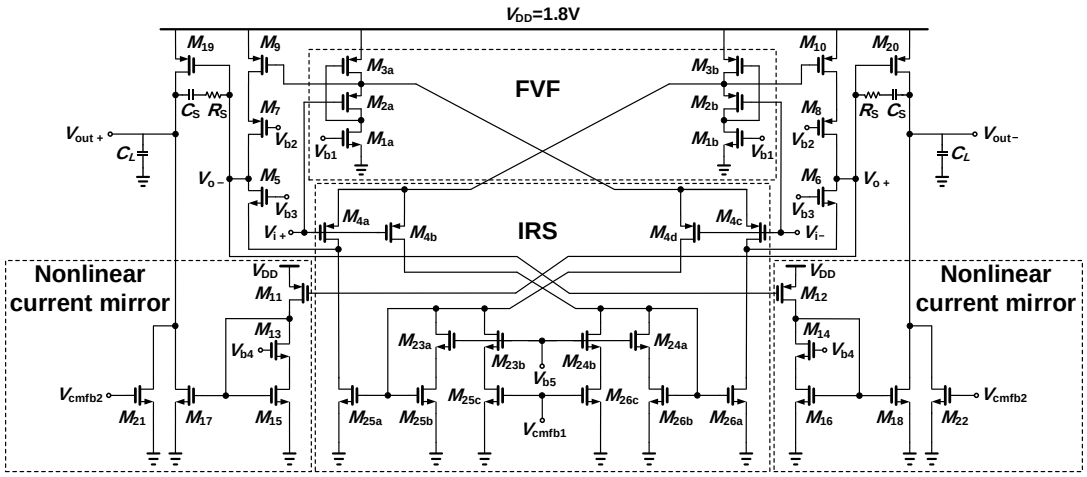


Fig. 3: Schematic of the two-stage RFC amplifier [29].

Table 1: Dimensions of transistors and passive components in the OTA design

Parameter	Value	Parameter	Value
$(W/L)_{1a,1b}$	1×5µm/0.18µm	$(W/L)_{19,20}$	2×40µm/0.36µm
$(W/L)_{2a,2b}$	1×25µm/0.18µm	$(W/L)_{21,22}$	2×10µm/0.36µm
$(W/L)_{3a,3b}$	50µm/0.18µm	$(W/L)_{23a,24a}$	2µm/0.18µm
$(W/L)_{4a,4b,4c,4d}$	1×12.5µm/0.18µm	$(W/L)_{23b,24b}$	0.8µm/0.18µm
$(W/L)_{5,6}$	1×30µm/0.18µm	$(W/L)_{25a,26a}$	6×2µm/0.18µm
$(W/L)_{7,8}$	1×60µm/0.18µm	$(W/L)_{25b,26b}$	2µm/0.18µm
$(W/L)_{9,10}$	1×60µm/0.18µm	$(W/L)_{25c,26c}$	0.8µm/0.18µm
$(W/L)_{11,12}$	2×40µm/0.36µm	C_S	30 pF
$(W/L)_{13,14,15,16}$	2×10µm/0.36µm	C_L	100 pF
$(W/L)_{17,18}$	2×10µm/0.36µm	R_S	500Ω

Furthermore, the POF curve illustrating the relationship between inference time and accuracy, is depicted in Fig. 4, providing valuable insights into the trade-offs between computational efficiency and prediction reliability.

Subsequently, the routing process has been carried out using the proposed SA-NSGA3-based approach. Figure 5 illustrates an example of routing where the SA algorithm has not been applied. As observed in this figure, the routing is not performed efficiently. For instance, an unnecessary layer transition occurs (shown by yellow), highlighting the limitations of the non-optimized approach. Unnecessary layer transitions lead to an excessive number of vias, which not only increase parasitic resistance and capacitance but also degrade the overall performance of the amplifier. This can result in signal integrity issues, higher power consumption, and reduced frequency response, ultimately affecting the circuit's efficiency.

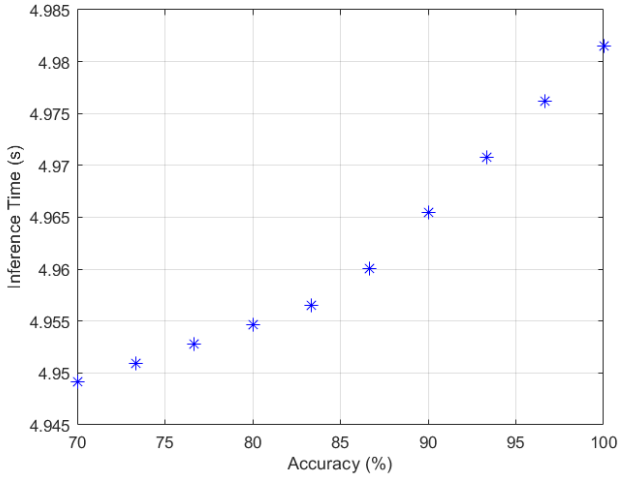


Fig. 4: POF Depicting the Trade-off Between Inference Time and Accuracy in the Proposed CNN-Based Approach.

Figure 6 illustrates an example of routing using the proposed SA-NSGA3 method. As shown in this figure, routing can be effectively performed with fewer iterations, highlighting the high efficiency of the algorithm in achieving optimal results in a reduced number of iterations. This reduction in the number of iterations translates to decreased computational time and faster routing processes without compromising the quality of the final routing. This feature is particularly advantageous in complex designs where time and computational resources are limited, and it can significantly contribute to the overall optimization of system performance.

Finally, the layout of the two-stage RFC amplifier has been fully completed using the proposed SA-NSGA2 method. The result is presented in Fig. 7. The layout area of the two-stage RFC amplifier is equal to $141\mu m \times 165\mu m$. Here, the number of layers in the routing step is equal to 2. The Bode diagrams of the two-stage RFC amplifier are presented in Fig. 8, demonstrating a remarkable DC-gain of 104.5 dB. This high DC-gain is indicative of the amplifier's excellent low-frequency performance. Additionally, the amplifier exhibits a unity-gain bandwidth (UGBW) of 40 MHz, which reflects its capability to maintain performance across a broad range of frequencies.

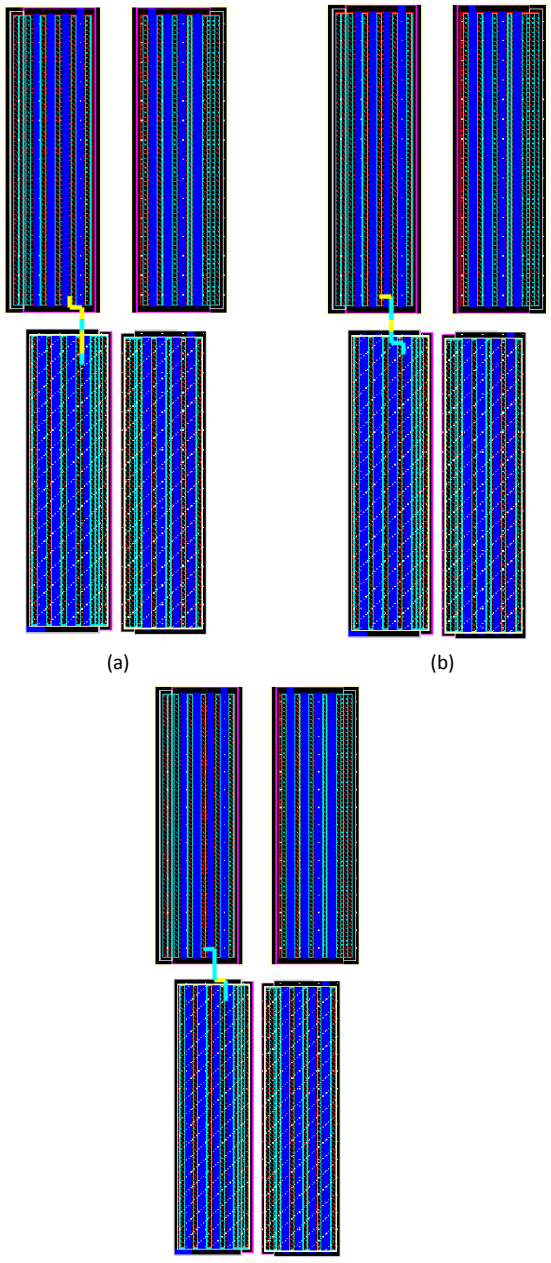


Fig. 5: Illustration of the routing progress using only NSGA-III: (a) Routing after 5 Iterations, (b) Routing after 10 iterations, (c) Placement result after 20 iterations.

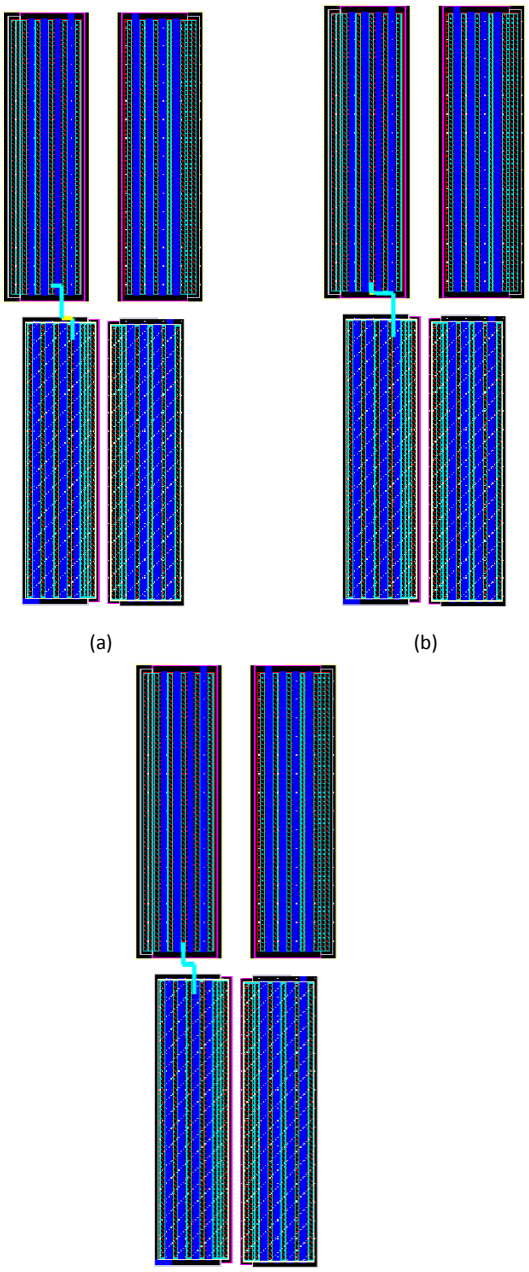


Fig. 6: Illustration of the routing progress using SA-NSGA3: (a) Routing after 5 iterations, (b) Routing after 10 iterations, (c) Placement result after 20 iterations.

The phase margin of 73° further underscores the stability of the amplifier, ensuring reliable operation without risk of oscillation. These performance metrics highlight the robustness of the two-stage RFC amplifier, making it suitable for high-precision applications requiring both high gain and stability. To provide a more comprehensive evaluation of the dynamic behavior, the step response of the circuit has been added in Fig. 9. The simulation is performed with an input amplitude of 1 V peak-to-peak and a frequency of 2 MHz. The training curves of the CNN are presented in Fig. 10. As the training progresses, the accuracy steadily increases, demonstrating that the network is effectively learning to classify the input data. Simultaneously, the loss decreases consistently across epochs, indicating that the model is minimizing the prediction errors and converging toward an optimal solution. These trends reflect the stability of the training process and suggest that the network is not overfitting, as the loss reduction corresponds with improved accuracy. Overall, the curves confirm that the CNN is successfully adapting its parameters to achieve high performance on the given task.

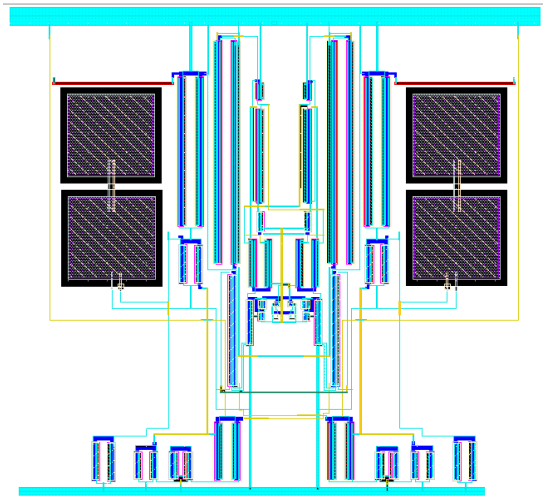


Fig. 7: The final layout after routing.

Table 2 presents a comparison of the post-layout simulation results of the proposed method with those of the existing method [32]. This Table reports the mean and variance of key specifications for the proposed comparator over four independent runs. The results indicate that the DC-gain, runtime, layout area, and area utilization are consistent, demonstrating reliable performance. Reporting both mean and variance highlights the stability and reproducibility of the proposed approach. The proposed method, leveraging the CNN-based placement technique and hybrid SA-NSGA3 routing, results in a significantly more compact layout compared to the conventional method. The CNN-based placement allows for more efficient utilization of the available space by automatically optimizing the positioning of components based on symmetry and proximity constraints. Additionally, the hybrid routing approach, combining the strengths of SA and NSGA3, ensures that the routing is not only efficient but also minimizes the use of unnecessary vias and excessive layer transitions. As a result, the method achieves better area utilization, leading to a more efficient and cost-effective design with improved performance characteristics. This compactness in layout contributes to reducing overall chip size while maintaining high functionality and signal integrity.

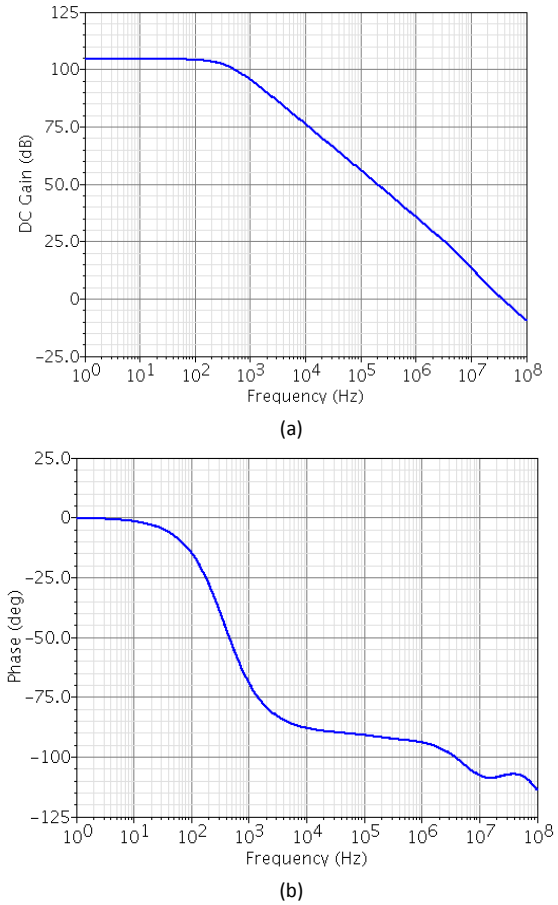


Fig. 8: Bode diagrams of the OTAs: (a) Amplitude Response, (b) Phase Response.

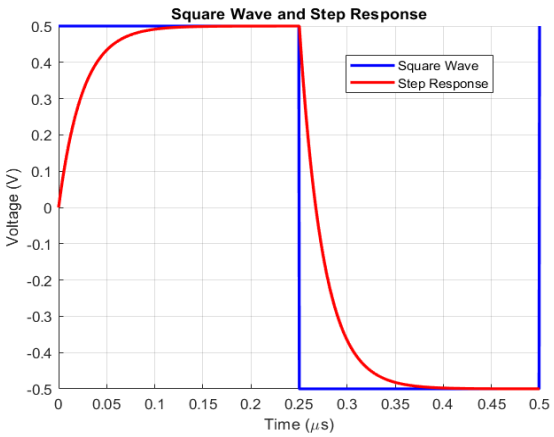


Fig. 9: Square wave and step response.

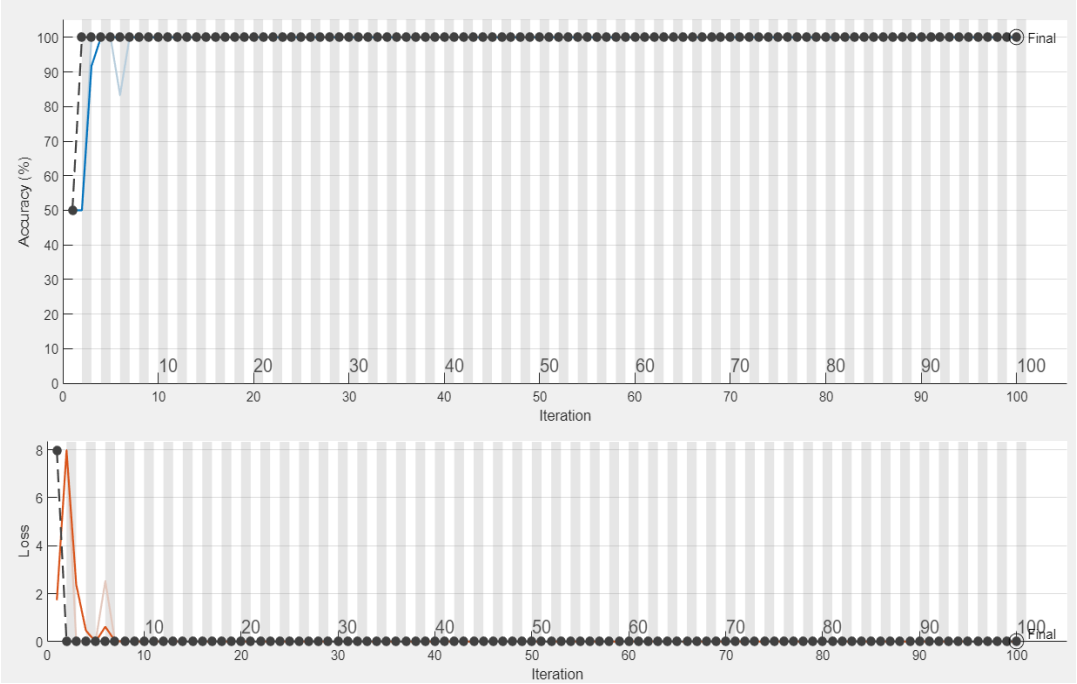


Fig. 10: The Accuracy and loss of the CNN.

Table 2: Comparison of post-layout simulation results between the proposed method and the existing method

No.	Specifications	Post-layout performance		
		This work		[32]
		Mean	Variance	
1	DC-gain (dB)	104.5	0.95	101.2
2	Total runtime (s)	1088	25.4	1134
3	Layout Area (mm^2)	0.023	0.001	0.025
4	Area Utilization (%)	84	1.8	78

To address the concern regarding generalizability, the proposed methodology was evaluated not only on the two-stage RFC amplifier but also on a dynamic comparator [33]. The circuit under test is illustrated in Fig. 11.

The clock signal is shown in Fig. 12(a), the input signal in Fig. 12(b), and the comparator output in Fig. 12(c), clearly demonstrating the correct operation of the comparator.

Furthermore, Table 3 presents a comparison between the proposed method and the reference design, indicating that the proposed approach achieves acceptable and competitive results compared to the existing method.

In the proposed method, the layout area is 5.8 µm × 10.1 µm.

The average propagation delay is 95.1 ps, and the average dynamic power is 4.83 µW, resulting in a power-delay product (PDP) of approximately 0.459 fJ. The offset voltage is 6.2 mV. It should be emphasized that these results are obtained from post-layout simulations, reflecting the effects of parasitics and realistic layout constraints.

Table 3: Post-layout evaluation of the proposed method versus existing approaches for dynamic comparator

No.	Specifications	Post-layout performance	
		This work	[33]
1	Average Delay (ps)	95.1	93.4
2	Average Dynamic Power (µW)	4.83	4.72
3	PDP (fJ)	0.46	0.44
4	Layout Area (µm2)	58.6	--

The POF for the proposed comparator (Fig. 13), considering parasitic effects, shows that a slight increase in delay results in a reduction of dynamic power,

indicating efficient utilization of current and timing. In comparison, the comparator reported in [33], without parasitic consideration, exhibits slightly lower delay and power, but parasitic effects are not accounted for. Therefore, the proposed method provides a more accurate and realistic representation of the delay–power trade-off.

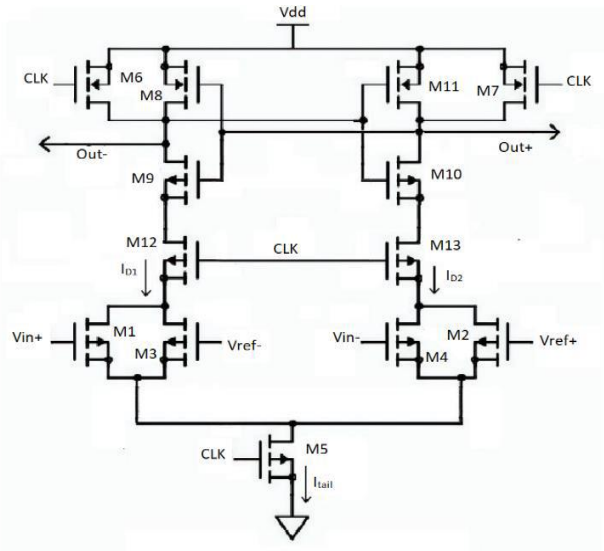
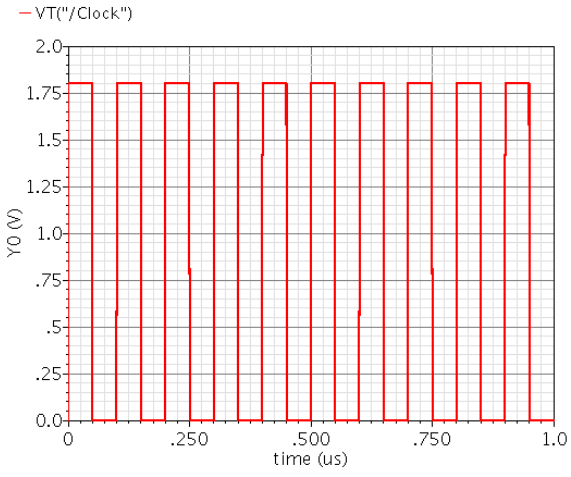


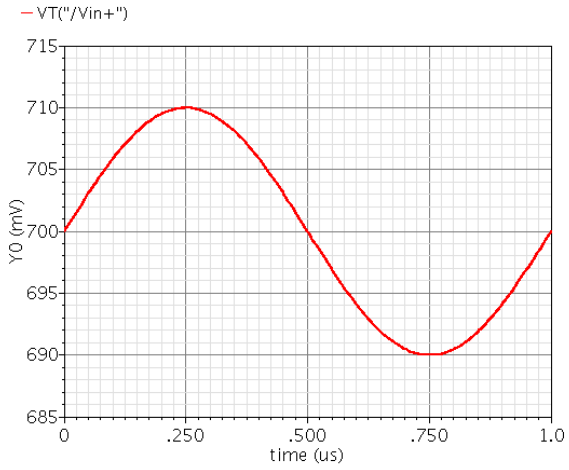
Fig. 11: Dynamic latch comparator [33].

The results of this additional study confirmed that the presented framework—consisting of constraint extraction using CNN, optimization via NSGA-III, and hybrid routing—can be effectively applied not only to amplifier designs but also to other analog circuit topologies.

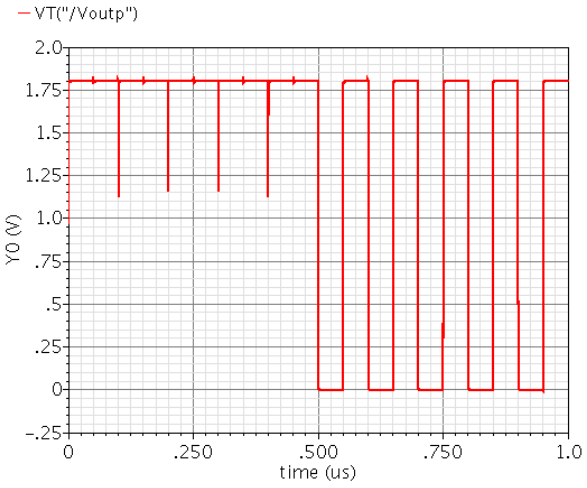
The investigations on the dynamic comparator further verified that the proposed method preserves the ability to generate compact layouts while satisfying symmetry and proximity constraints, thereby improving circuit performance. These findings demonstrate the scalability and robustness of the proposed approach in handling diverse analog and mixed-signal circuit designs.



(a)



(b)



(c)

Fig. 12: Dynamic Comparator Results: (a) Clock signal, (b) Input signal applied to the dynamic comparator, (c) Output response.

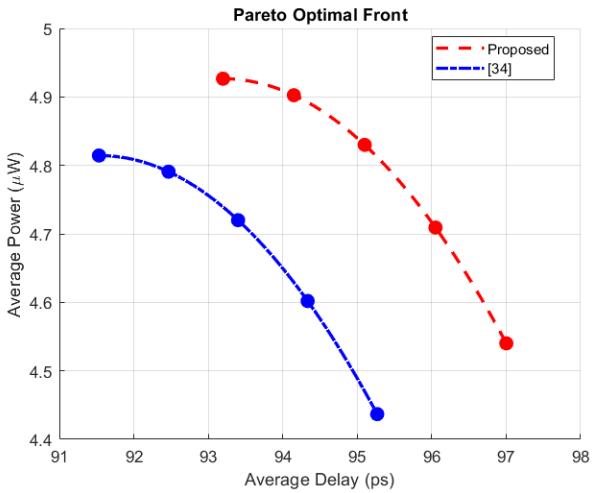


Fig. 13: POF of Dynamic Comparator.

Conclusion

This paper has demonstrated that the proposed

method for placement and routing in integrated systems, utilizing evolutionary algorithms and CNN, has effectively contributed to optimizing the performance of analog circuits.

The extraction of symmetry and proximity constraints using CNN and the optimization of its parameters via the NSGA-III algorithm have enabled the generation of a compact and efficient layout. Additionally, the hybrid routing approach, combining SA and NSGA-III, has enhanced the routing process and supported multi-objective optimization.

Simulation results for the two-stage recycling folded cascade (RFC) amplifier in 0.18µm CMOS technology with a 1.8V supply voltage have shown improvements in circuit performance and better utilization of physical resources.

This method has clearly offered advantages in design optimization and circuit performance enhancement over traditional approaches and can be applied to complex and industrial designs.

Author Contributions

Conceptualization and design, A. Gholami Boorkheyli; formal analysis, A. Gholami Boorkheyli; software, A. Gholami Boorkheyli; investigation, A. Gholami Boorkheyli, M. Babaeinik, H. Dehbovid. V. Ghods, ; writing—original draft preparation, A. Gholami Boorkheyli; writing—review and editing, M. Babaeinik, H. Dehbovid, V. Ghods. supervision, M. Babaeinik, H. Dehbovid, V. Ghods.

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Conflict of Interest

The authors declare no potential conflict of interest regarding the publication of this work. In addition, the ethical issues including plagiarism, informed consent, misconduct, data fabrication and, or falsification, double publication and, or submission, and redundancy have been completely witnessed by the authors.

Abbreviations

CNN	Convolutional Neural Network
NSGA-III	Non-Dominated Sorting Genetic Algorithm III
RFC	Recycling Folded Cascade
UGBW	Unity-Gain Bandwidth
OTA	Operational Transconductance Amplifier
SA	Simulated Annealing
IC	Integrated Circuit
CLB	Configurable Logic Block

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