Journal of Electrical and Computer Engineering Innovations
(JECEI)
Journal homepage: http://www.jecei.sru.ac.ir

Research paper

A Second Generation Current Conveyor Employing a Flipped Voltage Follower and Improved DC Voltage Gain Operational Transconductance Amplifier

E. Tavassoli [1], *S. M. Anisheh* [1,*], *M. Radmehr* [1]

Department of Electrical Engineering, Sari Branch, Islamic Azad University, Sari, Iran.

Article Info

Article History:
Received 04 November 2024
Reviewed 20 January 2025
Revised 26 February 2025
Accepted 09 March 2025

Keywords:
Current-mode circuit
Second generation current conveyor
Flipped voltage follower
Operational amplifier

*Corresponding Author's Email Address:
s.m.anisheh@ee.kntu.ac.ir

Abstract

Background and Objectives: The background of this research is the significance of current conveyors as essential building blocks in current-mode circuits. The objective is to design and simulate a second generation current conveyor (CCII) in a 180-nm CMOS process, aiming to achieve low impedance, accurate voltage copying, and high DC voltage gain.

Methods: The proposed CCII design utilizes a flipped voltage follower (FVF) to provide low impedance. A novel operational transconductance amplifier (OTA) is introduced to accurately copy the voltage within the circuit. This OTA employs a positive feedback technique to increase its output resistance, thereby enhancing DC voltage gain and reducing input impedance. The performance of the presented CCII is evaluated through simulations in a 180-nm CMOS technology using Cadence software.

Results: The simulation results show the successful operation of the CCII circuit. Key performance metrics include voltage and current tracking errors of 0.3% and 0.1%, respectively, and a bandwidth of 1.4 GHz.

Conclusion: The research concludes that a new OTA and CCII have been successfully simulated in a 180-nm CMOS process. The proposed CCII design, based on FVF and a novel OTA with positive feedback, achieves improved DC voltage gain without compromising other specifications like power consumption, UGBW, and stability. The tracking errors in the proposed method are lower compared to existing approaches.

Introduction

Analog signal processing can be achieved through either voltage-mode or current-mode techniques. Voltage-mode circuits typically experience a fixed bandwidth product, which results in a decrease in amplifier bandwidth as voltage gain increases [1]. To address this issue, various approaches have been suggested to surmount the gain-dependent bandwidth constraint. One promising approach involves utilizing current-mode devices, which are capable of operating at high frequencies. While voltage-mode circuits have been widely used, current-mode circuits have emerged as a promising alternative due to their inherent advantages. These include a higher slew rate (SR), a wider operating frequency range, and a bandwidth that remains constant across various gain levels [3].

Current conveyors are regarded as fundamental components in current-mode circuits. These versatile analog components have garnered significant attention from researchers [3], [4]. They are characterized as three-port structures. When the ports are labeled X, Y, and Z, the following equation describes their behavior:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & M & 0 \\ 1 & 0 & 0 \\ 0 & N & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

where in (1), I and V represent the currents and voltages

at the respective nodes. This discussion focuses on the second generation current conveyor (CCII), where the value of M is zero. An ideal CCII exhibits the following characteristics:

- High impedance at node Y, low impedance at node X, and high output impedance at node Z.
- Precise voltage transfer from node Y to node X and current transfer from node X to node Z.
- High speed performance for a specified bias current.
- Low operating supply voltage.

Several CCII implementations have been proposed in the literature [3]-[10]. In [3], a current-mode instrumentation amplifier using a fully differential operational floating conveyor (FD-OFC) is presented. The FD-OFC enhances design flexibility and noise rejection, requiring only one circuit for simplicity and low-voltage operation (1.2 V). The design is analyzed analytically and simulated in 130-nm technology using Cadence software.

References [4] and [5] introduce the operational floating current conveyor (OFCC) and discuss its applications. The OFCC operates efficiently with a 1.2V supply voltage and offers a wider bandwidth. It consists of two CCII blocks, a non-inverting trans-impedance amplifier, and a current steering circuit. The CCII includes a unity-gain amplifier followed by a common source amplifier [6]. In the first CCII, voltage tracking occurs between nodes Y and X, while current tracking is performed between nodes W and Z in the second CCII. This approach provides high performance using a simple circuit topology, but the resistance at terminal X of the CCII can be relatively high.

Reference [7] explores three realizations of the OFC. The first realization employs two CCII blocks and a non-inverting trans-impedance amplifier. The second OFC uses a CCII block, a non-inverting trans-impedance amplifier, and a positive current follower. The third OFC configuration includes a CCII block, an inverting trans-impedance amplifier, and a positive current follower. However, these realizations require a lower impedance at terminal X and a voltage gain closer to unity.

Reference [8] presents a digitally controlled OFCC-based filter, incorporating a trans-conductance amplifier and a bandpass filter to reduce power consumption. However, this approach has a limited bandwidth. A CMOS OFCC structure suitable for instrumentation amplifiers is proposed in [9], designed in 90-nm process. While it reduces power consumption, the bandwidth improvement is not significant. Reference [10] introduces a logarithmic amplifier based on the OFCC, comprising an OFCC, a diode, and a grounded resistor. The CCII CMOS circuit uses a cascade current mirror to increase output impedance, but the low impedance condition at node X is not fully achieved.

This paper proposes a new CMOS CCII with improved specifications, including low voltage and current tracking errors and high bandwidth. The proposed CCII utilizes a FVF to achieve low impedance at node X. A novel OTA is introduced to accurately copy the voltage from node Y to node X. By employing positive feedback, the OTA's output resistance and DC voltage gain are increased, further reducing the impedance at node X and increasing the input impedance at node Y.

The subsequent sections of this article are organized as follows. Initially, the circuit structure of the presented OTA and CCII will be discussed in detail. Next section presents the simulation results and compares them to existing works. To wrap up, the key findings of the research presented will be summarized.

Proposed Circuits

In this section, the proposed circuits of OTA and CCII are explained and the theoretical analysis are presented.

Proposed OTA

OTAs are fundamental components in numerous analog and mixed-mode circuits [11]-[16]. The conventional OTA circuit was first introduced in [17]. The presented OTA is illustrated in Fig. 1. Nodes V_O and V_{out} represent the outputs of the first and second stages, respectively. The input differential pair comprises transistors M_1 and M_2, biased by the FVF circuit. The FVF is capable of operating with low supply voltages [18]-[20]. M_{2a}, M_{2b}, M_{3a}, and M_{3b} devices, in conjunction with M_{1a} and M_{1b} transistors acting as current sources, constitute the FVF. This structure incorporates two additional signal amplification paths.

In the first path, the source of M_2 device is connected to the gate of M_9 transistor using the FVF. Additionally, there is a path connecting the source of M_1 to the gate of M_{10}. Consequently, the input signal is present at the gate-source of M_9 and M_{10}, increasing the first-stage transconductance from $g_{m1,2}$ to $g_{meff1} = g_{m1,2} + g_{m9,10}$. This enhancement leads to an improvement in DC voltage gain.

FVF-based nonlinear current mirrors (NLCM), consisting of M_{11}, M_{15}, M_{17}, M_{19} transistors and M_{12}, M_{14}, M_{16}, M_{18} devices, are used in the second stage to improve the SR. As depicted in Fig. 1, the gate of M_{11} is connected to V_{O+}, and similarly, the gate of M_{12} is connected to V_{O-}. This connection provides an additional signal amplification path by increasing the second-stage transconductance.

This paper modifies the OTA structure described in [17] to boost DC voltage gain without impacting power consumption. The output resistance of the second stage is improved by employing positive feedback, which leads to an increased DC voltage gain. Transistor pairs (M_{23}, M_{24}) and (M_{25}, M_{26}) are added to the conventional structure as current sources.

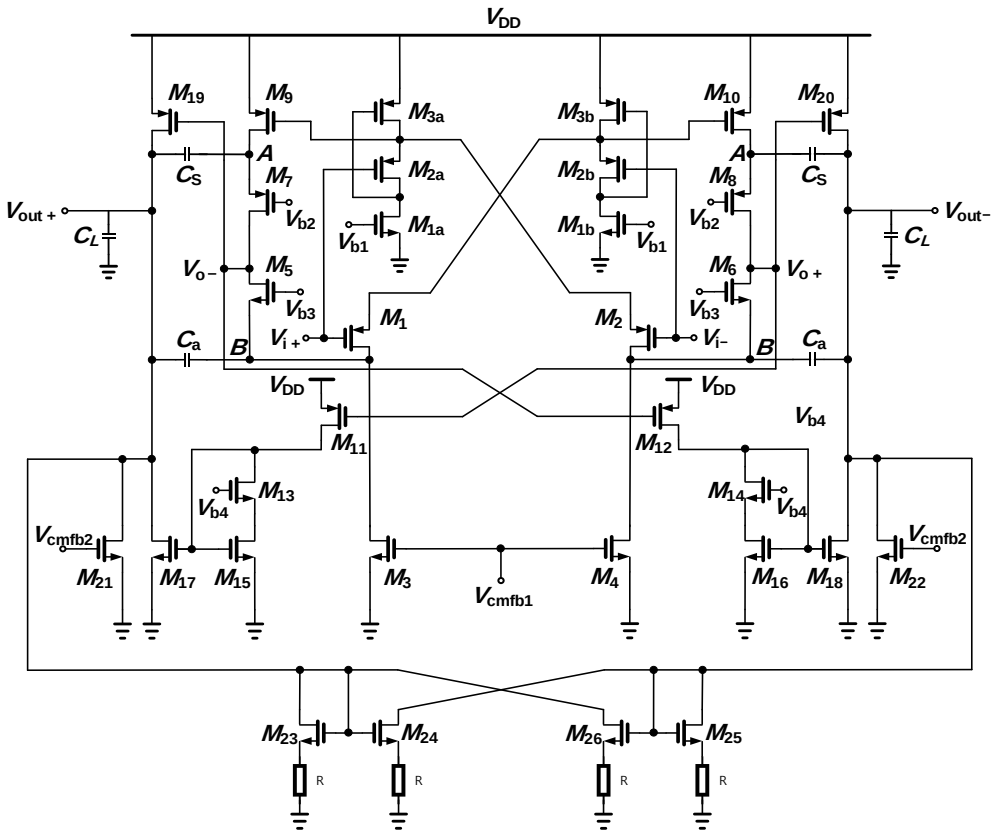


Fig. 1: The proposed OTA.

Positive feedback is established by connecting these current sources to the outputs [21]. The DC voltage gain of the suggested OTA is determined as follows:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & M & 0 \\ 1 & 0 & 0 \\ 0 & N & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

$$A_d = A_1 \times A_2 \quad (2)$$

where A_1 is the DC voltage gain of the first stage and it can be obtained as below:

$$A_1 = G_{meff1} R_{out1} \quad (3)$$

and,

$$R_{OUT1} = g_{m7} r_{ds7} r_{ds9} \| \left(g_{m5} r_{ds5} (r_{ds1} \| r_{ds3}) \right) \quad (4)$$

A_2 represents the DC voltage gain of the second stage and is calculated as follows:

$$A_2 = G_{meff2} R_{out2} \quad (5)$$

where,

$$G_{meff2} = g_{m19+} g_{m11} g_{m17} (r_{ds11} \| r_{ds13}) \quad (6)$$

$$R_{out2} = \frac{1}{g_{ds17} + g_{ds19} + g_{ds21} + G_{cs}} \quad (7)$$

$$G_{cs} = \frac{1}{\frac{g_{m26} r_{ds26} R + r_{ds26} + R}{1 - g_{m26} r_{ds26}}} + \frac{g_{m23}}{1 + g_{m23} R} \quad (8)$$

In the above equations, R_{out} refers to the output resistance of each stage. g_m is the transconductance of a NMOS/PMOS device. Moreover, r_{ds} is the resistance of the drain-source of the utilized transistors, $g_{ds}=1/r_{ds}$, and $G_{cs}=1/R_{cs}$. R_{cs} is the resistance of the current source seen from the node V_{out+} and it can be calculated according to Fig. 2. If the denominator of (7) is close to zero but its value is positive, then the differential gain increases significantly and the system is stable.

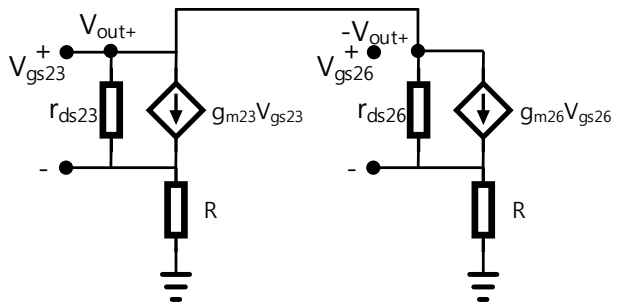


Fig. 2: Equivalent small-signal model for calculating the output resistance of the current source.

Proposed CCII

The proposed CCII structure is depicted in Fig. 3. The set of NMOS devices (M_1, M_2, and M_3), and PMOS devices (M_4, M_5, M_6) form the FVF. Transistor M_7 works as a reference current generator. (M_1, M_4, M_8) is a FVF circuit.

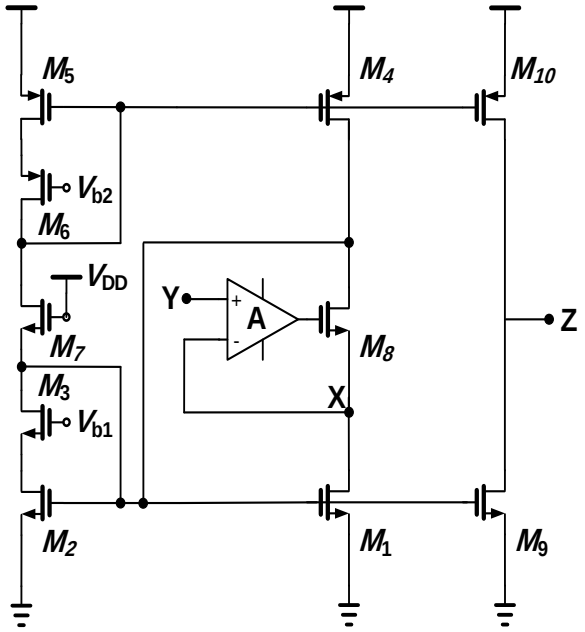


Fig. 3: The proposed CCII based on the OTA.

The choice of using a FVF in the proposed CCII offers several key advantages over traditional configurations.

1- Low Impedance: The FVF structure inherently provides low output impedance, which is crucial for ensuring proper current transfer and minimizing signal distortion in current-mode circuits. This low impedance directly contributes to the improved performance of the CCII, especially in driving high-frequency loads.

2- Enhanced Voltage Tracking: The FVF configuration helps in accurate voltage tracking by reducing the mismatch between the input and output voltages. This is particularly beneficial for achieving the precise replication of the input voltage in the CCII structure.

3- Impact on Performance: By using FVF, we can significantly enhance the performance in terms of bandwidth and DC gain. The low impedance provided by the FVF ensures that the circuit can operate at higher speeds and with greater precision, resulting in an overall improvement in the CCII's voltage and current tracking capabilities.

The operational amplifier with gain A is the amplifier shown in Fig. 1, which is used for three purposes. First, the voltage of nodes X and Y should be close to each other. Second, the resistance at the X node should be reduced. Finally, the resistance at the Y is high. The transistors (M_9, M_{10}) are used in CCII output.

From Fig. 3, it can be seen that the input impedance of the Y node is infinite. The output impedance of node X is equal to:

$$R_x = \frac{1}{A_d g_{m1} g_{m8} (r_{ds4} \| r_{ds8})} \quad (9)$$

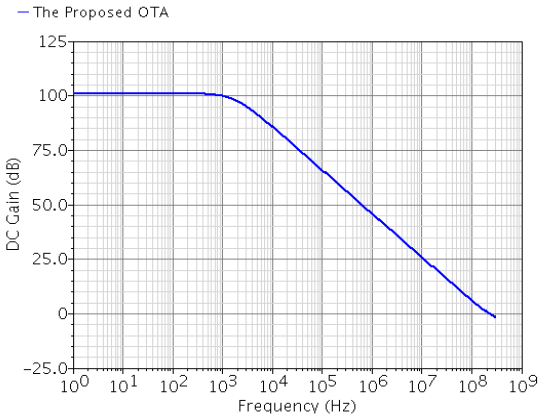
The above equation shows that as the Ad increases, the resistance at node X decreases. The output resistance in node Z is obtained from the following equation.

$$R_z = r_{ds9} \| r_{ds10} \quad (10)$$

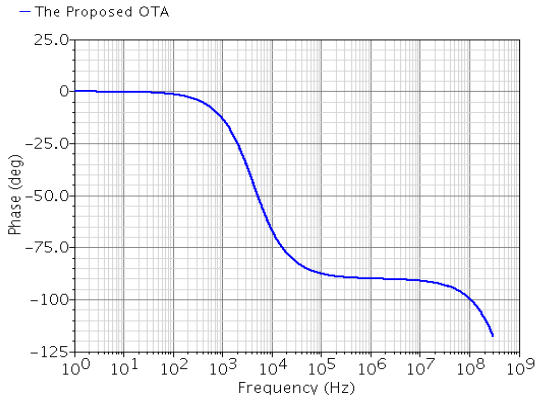
Simulation Results

Both the presented OTA and CCII are simulated in a standard 180-nm CMOS process with a supply voltage of 1.8 V. The component values are similar to those used in the OTA presented in [17]. For the CCII, the dimensions of the transistors are as follows: the NMOS has dimensions of 1.5µm / 0.18µm, and the PMOS has dimensions of 3.6µm / 0.18µm. Fig. 4 illustrates the open-loop frequency responses of the OTA. The DC voltage gain is measured at 101 dB, representing an enhancement of 7 dB over the traditional structure. The OTA's unity-gain bandwidth (UGBW) is 230 MHz, and its phase margin is 61°, indicating circuit stability.

Monte-Carlo (MC) simulations of the OTA were conducted to assess process and mismatch variations. Fig. 5 shows the MC histograms of the designed amplifier based on 1000 simulation runs. The mean and standard deviation values for the DC voltage gain are 104.2 dB and 7.4 dB, respectively. Similarly, the mean and standard deviation values for the phase margin are obtained 66.6 and 1.1 degrees, respectively.

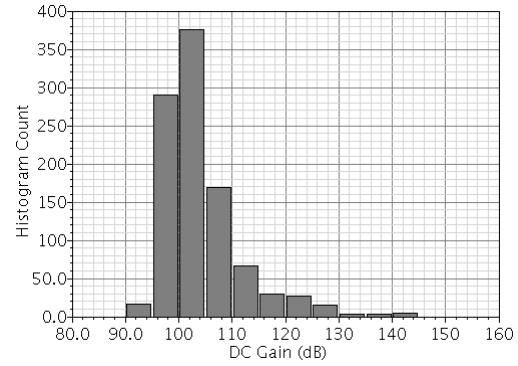


(a)

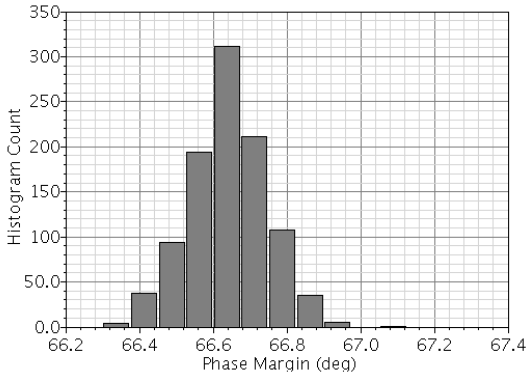


(b)

Fig. 4: The open-loop frequency response of the designed OTA: (a) DC voltage gain, (b) phase response across the frequency range.



(a)



(b)

Fig. 5: Histogram of Monte Carlo (MC) simulation results for the proposed OTA: (a) DC voltage gain, (b) phase margin.

Table 1: A comparative analysis of the developed amplifier's performance versus existing design, highlighting the improvement in voltage gain

Parameter	This work	[17]	[19]
Technology (nm)	180	180	180
Supply Voltage (V)	1.8	1.8	1.8
DC Voltage Gain (dB)	101	93	84
Input-Referred Noise@100kHz $(\mu v/\sqrt{Hz})$	0.32	0.31	0.34
Silicon Area (mm²)	0.022	0.021	0.07
Differential Output Swing (V_{pp})	2.8	2.8	2.8
Phase Margin (^{o})	62	65	77
Power Dissipation (mW)	2.8	2.8	3.1
SR (V/µs)	650	494	63
UGBW (MHz)	230	216	91
Load Capacitor (pF)	1	1	100
Operating Region	Strong Inversion	Strong Inversion	Strong Inversion
FOM_S (MHz×pF/mA)	147	138	5290
FOM_L (V×pF/µs×mA)	417	316	3660

Table 1 presents the post-layout simulation results for the designed OTA and its competitor. The proposed OTA exhibits a higher DC voltage gain compared to the other solution, while maintaining comparable parameters such as UGBW, power consumption, and stability. To evaluate the relative performance of the two competitors, the figures of merit described in (11) and (12) are utilized [22]-[30].

$$FOM_S = \frac{UGBW\ C_L}{I_T} \quad (11)$$

$$FOM_L = \frac{SR\ C_L}{I_T} \quad (12)$$

where I_T is the total circuit current and C_L is the load capacitor. From Table 1, it can be concluded that the figure of merit of the presented OTA is better.

The total power consumption of the proposed CCII is 3.1 mW.

Fig. 6 illustrates the input voltage tracking of the CCII, with an error of 0.3%. Fig. 7 depicts the output current tracking I_z/I_x, with an error of 0.1% across process and temperature corners. The bandwidth in TT (27°C), FF (-40°C), and SS (90°C) is 1.1 GHz, 1.7 GHz, and 1.1 GHz, respectively.

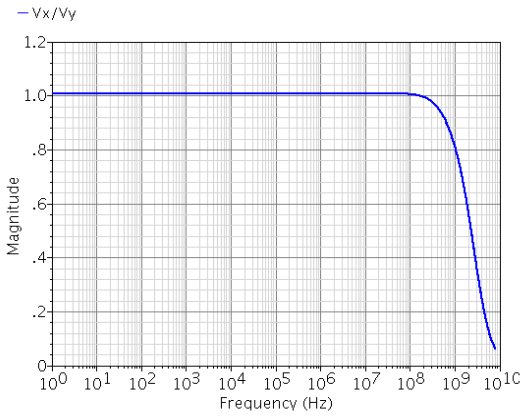


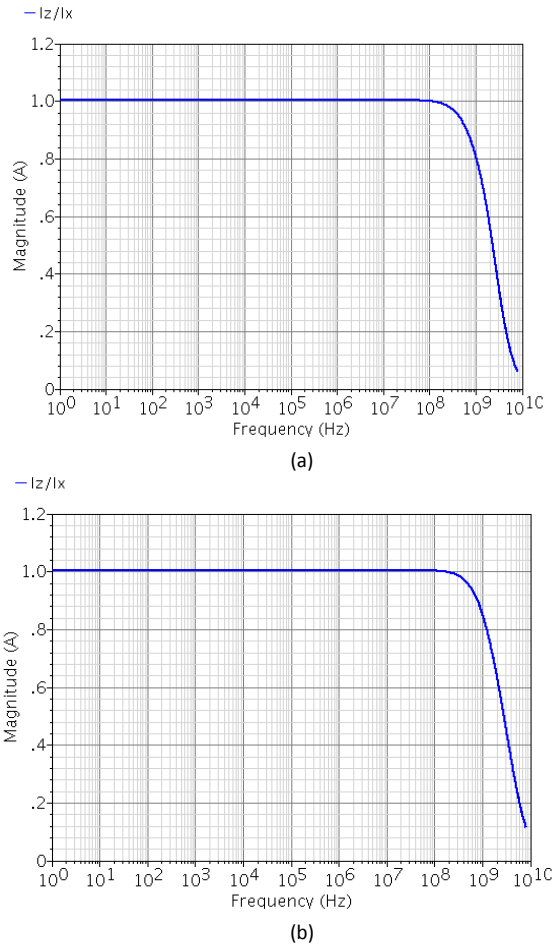
Fig. 6: Input terminals voltage tracking V_x/V_y. This figure illustrates the accuracy of voltage transfer between the terminal V_x and the terminal V_y.

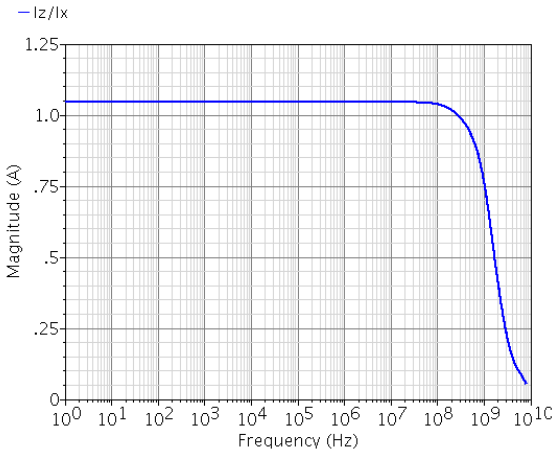
Table 2 presents a performance comparison between the designed CCII and one existing method. The results clearly demonstrate that the proposed method exhibits lower current and voltage tracking errors compared to existing approaches. Additionally, the proposed method offers a wider bandwidth than the existing methods. In [5] and [9], conventional methods are used in the CCII design to achieve certain performance metrics. However, the absence of positive feedback and innovative approaches in the OTA design leads to limitations in DC gain and other performance characteristics. In [18], a FVF is utilized, which affects the operating voltage. Compared to our design, this approach may not provide the optimal DC performance.

Table 2: Comparison of the performance between the developed design and existing similar works

References	This work	[5]	[9]	[18]
Process (nm)	180	130	90	500
Supply Voltage (V)	1.8	1.2	1.2	1.5
Input voltage tracking error (%)	0.3	0.%	-	-
Output current tracking error (%)	0.1	0.5	-	-
Bandwidth (GHz)	1.5	1.2	0.104	0.1
Power Consumption (mW)	3.1	1.5	3	0.6

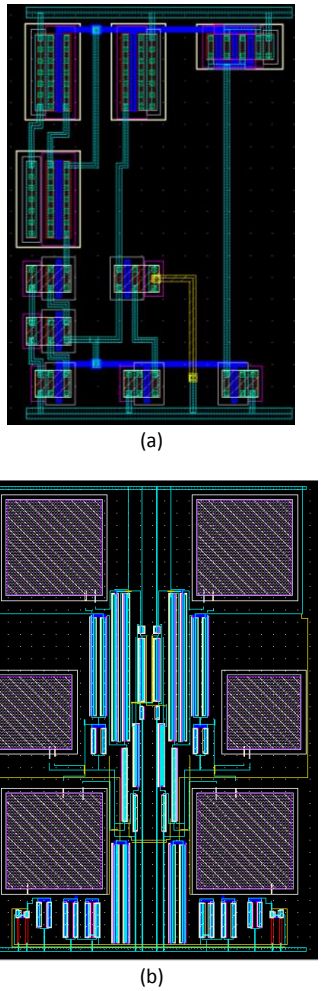
The layout view of the designed circuit is shown in Fig. 8. The physical dimension of the designed CCII is 12 µm x 17 µm, and the dimension of the designed OTA is 120 µm x 180 µm. These details provide a clearer understanding of the physical implementation and area utilization of the proposed design.





(c)

Fig. 7: Outputs current tracking I_z/I_x in different process corners and temperatures: (a) TT (27°C), (b) FF (-40°C), (c) SS (90°C). This figure shows the accuracy of current transfer in different operating scenarios.



(a)

(b)

Fig. 8: Layout view of the proposed design: (a) Proposed CCII, (b) Proposed OTA.

Conclusion

Current conveyors are essential components in many current-mode circuits. This paper presents a novel OTA and CCII designed in a 180-nm CMOS process. The

presented circuits operate at a supply voltage of 1.8 V. The designed CCII employs a FVF to achieve low impedance at node X. A new OTA is introduced to accurately copy the voltage within the circuit. The proposed OTA utilizes positive feedback to increase its output resistance, resulting in improved DC voltage gain. Simulations were conducted to evaluate the performance of the designed CCII. The DC voltage gain of the OTA was increased by approximately 7 dB compared to its competitor without affecting specifications such as power consumption, UGBW, and stability.

The current and voltage tracking errors in the proposed method are lower than those of existing methods. The proposed CCII design, with its low impedance and accurate voltage copying features, can be utilized in filter circuits, analog and digital signal processing, and signal amplification in telecommunications systems.

These features ensure that signals are transmitted with minimal attenuation and distortion, improving overall system performance.

Author Contributions

Conceptualization and design, E. Tavassoli; formal analysis, E. Tavassoli; software, E. Tavassoli; investigation, S. M. Anisheh.; writing—original draft preparation, E. Tavasolli; writing—review and editing, S. M. Anisheh. supervision, S. M. Anisheh, and M. Radmehr.

Conflict of Interest

The authors have disclosed that there are no potential conflicts of interest related to the publication of this work.

Acknowledgment

The authors would like to also express their gratitude to Alireza Ghorbani for his technical assistance and support, and for useful discussions and hints.

Abbreviations

MC	Monte-Carlo
OTA	Operational transconductance amplifier
CCII	Second generation current conveyor
FVF	Flipped voltage follower
SR	Slew rate
FD-OFC	Fully differential operational floating conveyor
OFCC	Operational floating current conveyor
NLCM	Nonlinear current mirrors
UGBW	Unity-gain bandwidth

References

[1] K. C. Smith, A. Sedra, "The current conveyor—A new circuit building block," Proc. IEEE, 56(8): 1368-1369, 1968.

[2] G. Yun et al., "An ultrasound receiver with bandwidth-enhanced current conveyor and element-level ultrasound transmitter for ultrasound imaging systems," IEEE Solid-State Circuits Lett., 7: 98-101, 2024.

[3] M. Kumngern, F. Khateb, T. Kulej, "Low-voltage low-power differential difference current conveyor transconductance amplifier and its application to a versatile analog filter," IEEE Access, 12: 92523-92535, 2024.

[4] N. M. Edward, Y. H. Ghallab, H. Mostafa, Y. I. Ismail, "A CMOS based operational floating current conveyor and its applications," in Proc. IEEE International Conference on Electronics, Circuits, and Systems (ICECS): 494-495, 2015.

[5] N. M. Edward, Y. H. Ghallab, H. Mostafa, Y. I. Ismail, "A CMOS based operational floating current conveyor," in Proc. IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2015.

[6] G. Palmisano, G. Palumbo, "A simple cmos CCII+," Int. J. Circuit Theory Appl., 23(6): 599-603, 1995.

[7] H. M. Hassan, A. M. Soliman, "Novel cmos realizations of the operational floating conveyor and applications," J. Circuits Syst. Comput., 14(6): 1113-1143, 2005.

[8] D. Nand, N. Pandey, R. Pandey, S. Jindal, "Operational floating current conveyor based digitally controlled hearing aid," in Proc. 5th International Conference on Signal Processing and Integrated Networks (SPIN): 647-651, 2018.

[9] F. Elsayed, M. Rashdan, M. Salman "CMOS operational floating current conveyor circuit for instrumentation amplifier application," Int. J. Electr. Electron. Eng. Telecommun., 9(5): 317-323, 2020.

[10] N. Pandey, P. Tripathi, R. Pandey, R. Batra, "OFCC based logarithmic amplifier," in Proc. International Conference on Signal Processing and Integrated Networks (SPIN): 522-525, 2014.

[11] R. S. Assaad, J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," IEEE J. Solid-State Circuits, 44(9): 2535-2542, 2009.

[12] N. Ning, F. Yang, S. Zhiling, L. Rui, W. Shuangyi, "A low-sensitivity negative resistance load fully differential OTA under low voltage 40nm CMOS logic process," Chinese scientific papers: 1-7, 2010.

[13] A. Dabas, S. Kumari, M. Gupta, R. Yadav, "Design and analysis of class AB RFC OTA with improved performance," in Proc. 8th International Conference on Signal Processing and Communication (ICSC): 582-586, 2022.

[14] M. Anand, Anushree, J. Dhanoa, "Gain and gain-bandwidth enhancement of recyclic folded cascode OTA using floating voltage source," in Proc. IEEE Delhi Section Conference (DELCON): 1-5, 2022.

[15] C. Taol, L. Lei, Z. Chen, Z. Hong, Y. Huang, "A 50MHz bandwidth TIA based on two stage pseudo-differential OTA with cascode negative resistance and R-C compensation technique," in Proc. IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS): 1-4, 2022.

[16] S. Adibi, R. Rubino, P. Toledo, and P. Crovetti, "Design of an analog and of a digital-based OTA in flexible integrated circuit technology," in Proc. 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS): 1-4, 2022.

[17] S. M. Anisheh, H. Shamsi, "Two-stage class-AB OTA with enhanced DC gain and slew rate," Int. J. Electron. Lett., 5(4): 438-448, 2017.

[18] R. G. Carvajal et al., "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," IEEE Trans. Circuits Syst. I Regul. Pap., 52(7): 1276-1291, 2005.

[19] S. M. Anisheh, H. Abbasizadeh, H. Shamsi, C. Dadkhah, K. Y. Lee, "84 dB DC-gain two-stage class-AB OTA," IET Circuits Devices Syst., 13(5): 614-621, 2019.

[20] S. M. Anisheh, H. Abbasizadeh, H. Shamsi, C. Dadkhah, K. Y. Lee, "98-dB gain class-AB OTA with 100 pF load capacitor in 180-nm digital CMOS process," IEEE Access,7: 17772-17779, 2019.

[21] S. M. Anisheh, H. Shamsi, M. Mirhassani, "Positive feedback technique and split-length transistors for DC-gain enhancement of two-stage op-amps," IET Circuits Devices Syst., 11(6): 605-612, 2017.

[22] K. P. Ho, C. F. Chan, C. S. Choy, K. P. Pun, "Reversed nested Miller compensation with voltage buffer and nulling resistor," IEEE J. Solid-State Circuits, 38(10): 1735-1738, 2003.

[23] A. D. Grasso, G. Palumbo, S. Pennisi, "Advances in reversed nested miller compensation," IEEE Trans. Circuits Syst. I, Regul. Pap., 54(7): 1459-1470, 2007.

[24] V. Michal, "OTA slew-rate and bandwidth enhancement based on dynamic input-overdriven current mirror," in Proc. International Conference on Applied Electronics (AE): 1-4, 2023.

[25] P. Li, L. Luo, Q. Wei, "A CLASS AB operational transconductance amplifier (OTA) with a slew rate enhancement (SRE) auxiliary circuit," in Proc. 3rd International Conference on Communication Technology and Information Technology (ICCTIT): 20-23, 2023.

[26] S. L. Tripathi, B. Raj, S. Verma, V. Narula, S. Saxena, "High gain multistage CMOS amplifier design at 45nm technology node," in Proc. IEEE Devices for Integrated Circuit (DevIC): 237-242, 2023.

[27] S. Choudhary, R. Chowdhury, T. Sharma, "Comparative analysis of operational transconductance amplifiers (OTA) for biomedical applications," in Proc. International Conference on Circuit Power and Computing Technologies (ICCPCT): 1330-1334, 2023.

[28] R. Jayachandran, E. B. Kumaradhas, A. S, "Design of second order low pass filter using inverter-based CMOS operational transconductance amplifier (OTA) through gm/ID methodology," in Proc. IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON): 519-524, 2024.

[29] S. Nasabi, S. S. Kotbagi, S. Javalagi, M. M, R. R. Patgar, B. A. Gunhalkar, "Design of operational transconductance amplifier (OTA) for 1.2V bandgap reference (BGR)," in Proc. 4th International Conference on Intelligent Technologies (CONIT): 1-6, 2024.

[30] S. Dutta, R. Ranjan, P. Kumari, P. Sinha, R. K. Ranjan, D. K. Singh, "Operational transconductance amplifier (OTA) based dual mode Multiphase Oscillator," in Proc. 5th International Conference on Recent Trends in Computer Science and Technology (ICRTCST): 332-337, 2024.

Biographies

Emad Tavassoli received the M.S degree in Electrical Engineering (Electronic) from Islamic Azad University Science and Research Branch Tehran, Iran in 2013. He is currently a student of Electronic Engineering at Islamic Azad University, Sari branch. His research interests include bilayer graphene, differential operational floating conveyors.

- Email: emadtavassoli@gmail.com
- ORCID: 0009-0008-2515-4731
- Web of Science Researcher ID: MFK-2999-2025
- Scopus Author ID: NA
- Homepage: NA

Seyed Mahmoud Anisheh received the Ph.D. degree in Electrical Engineering (Electronics) from K.N. Toosi University of Technology, Tehran, Iran in 2017. His research interests include high performance Op-Amps, automatic analog circuit layout generation, RFIC, and signal processing.

- Email: s.m.anisheh@ee.kntu.ac.ir
- ORCID: 0000-0003-0982-8608
- Web of Science Researcher ID: MFK-3141-2025
- Scopus Author ID: NA
- Homepage: NA

Mehdi Radmehr was born in 1974 and received the B.Sc., M.Sc., and Ph.D. degrees in Electrical Engineering from University of Tehran, Tarbiat Modares, and Islamic Azad University, Science and Research campus, Tehran, Iran, in 1996, 1998, and 2006 respectively. He is a specializing in power electronics, motor drives and power quality. He has worked for Mazandaran Wood and Paper Industries as an advisor since 1997 before starting his Ph.D. study. He has joined the scientific staff of Islamic Azad University, Sari branch since 1998.

- Email: maradmehr@gmail.com
- ORCID: 0000-0003-1678-9758
- Web of Science Researcher ID: NA
- Scopus Author ID: NA
- Homepage: NA

How to cite this paper:
E. Tavassoli, S. M. Anisheh, M. Radmehr, "A second generation current conveyor employing a flipped voltage follower and improved DC voltage gain operational transconductance amplifier," J. Electr. Comput. Eng. Innovations, 13(2): 455-462, 2025.

DOI: 10.22061/jecei.2025.11326.795

URL: https://jecei.sru.ac.ir/article_2307.html